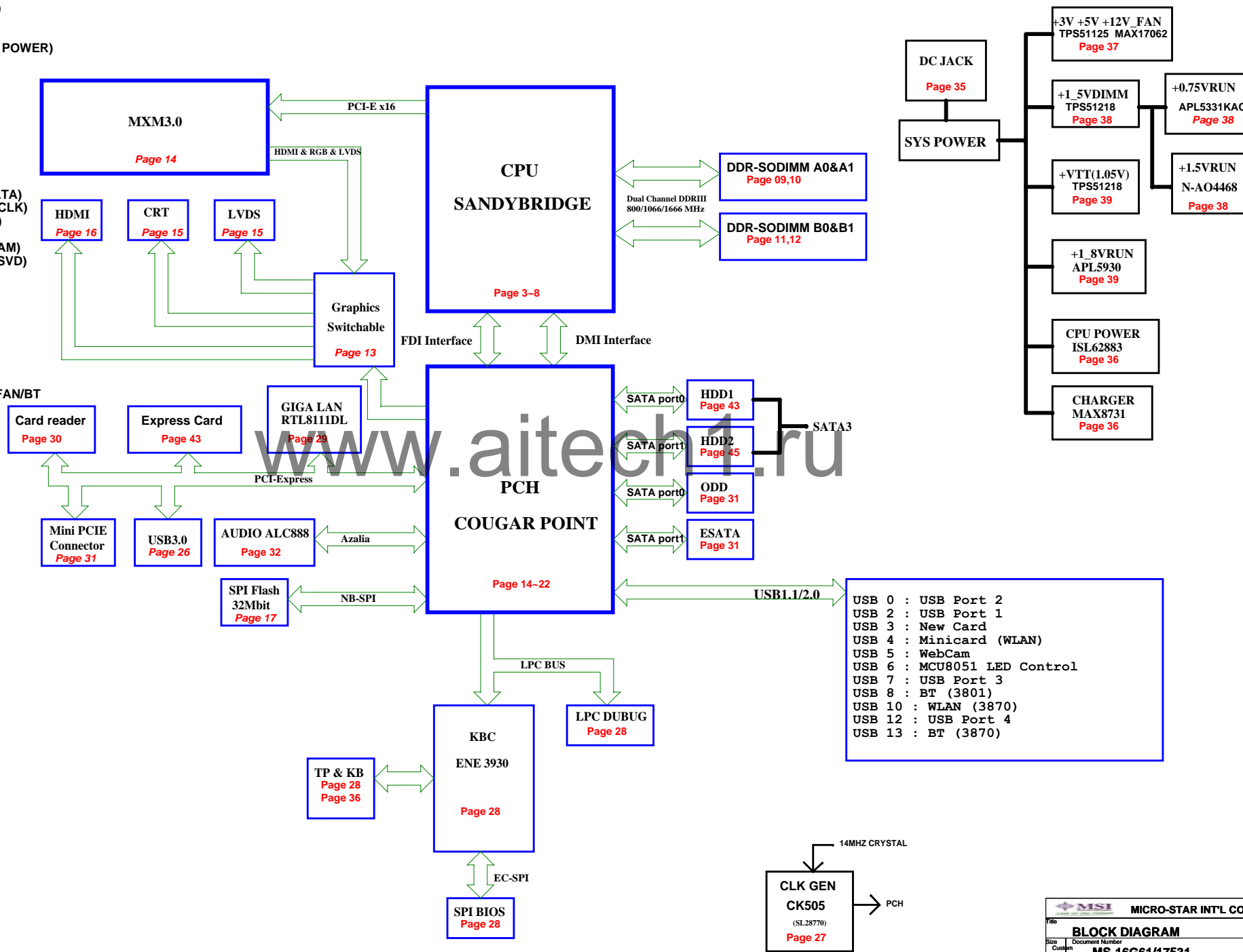


Huron River Platform

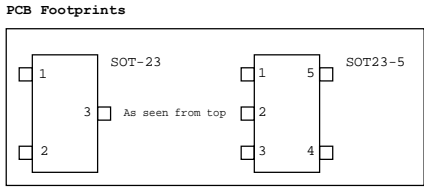
- 01 : BLOCK DIAGRAM
 02 : PLATFORM
 03 : PROCESSOR-1 (HOST BUS)
 04 : PROCESSOR-2 (DDR3)
 05 : PROCESSOR-3 (POWER)
 06 : PROCESSOR-4 (GRAPHICS POWER)
 07 : PROCESSOR-5 (GND)
 08 : PROCESSOR-6 (RESERVE)
 09 : DDR3 SODIMM A0
 10 : DDR3 SODIMM A1
 11 : DDR3 SODIMM B0
 12 : DDR3 SODIMM B1
 13 : SWITCH
 14 : MXM3.0 Slot
 15 : CRT/LVDS/CCD
 16 : HDMI
 17 : CougarPoint (HDA/JTAG/SATA)
 18 : CougarPoint (PCI-E/SMBUS/CLK)
 19 : CougarPoint (DMI/FDI/GPIO)
 20 : CougarPoint (LVDS/DDI)
 21 : CougarPoint (PCI/USB/NVRAM)
 22 : CougarPoint (GPIO/NCTF/RSVD)
 23 : CougarPoint (POWER)
 24 : CougarPoint (POWER)
 25 : CougarPoint (GND)
 26 : USB3.0
 27 : CLOCK GEN (SL28770)
 28 : KBC/EC/uP (KB3930)
 29 : GIGA LAN (RTL8111DL)
 30 : Card Reader (UB6250)
 31 : WLAN/TP/BT/USB
 32 : HDD2/ODD/ESATA Combo/FAN/BT
 33 : AUDIO(ALC888)
 34 : LED_8051
 35 : M_Battery select
 36 : M_Battery Charger
 37 : M_System Power
 38 : M_DIMM_1.5VRUN
 39 : M_VTT_1.8VRUN
 40 : M_CPU Power
 41 : M_0.8V
 42 : EMI/Screw
 43 : 16F1A_NewCard/HDD1
 44 : 16F1B_IO/Audio Board
 45 : 16F1C_HDD2
 46 : 16F1D_Cap Sensor Board
 47 : 16F1E_Touch Pad L/R Key
 48 : 16F1F_CDLED_RF
 49 : 16F1G_ABLED_Front
 50 : 16F1H_ABLED_L
 51 : 16F1I_ABLED_R
 52 : 16F1J_CDLED_L
 53 : 16F1K_CDLED_LF
 54 : PowerDown Sequence
 55 : PowerOn Sequence
 56 : History



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails			
POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	12V	S0, (S3-S5)	
+5VALW	5V	S0, (S3-S5)	
+5VRUN	5V	S0, S3	
+5VSUS	5V	S0	
+3VALW	3.3V	S0, (S3-S5)	
+3VRUN_CK505	3.3V	S0	Clock, MCH
+3VSUS	3.3V	S0, S3	
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0, (S3-S4)	DDR core
+1_5VSUS	1.5V	S0	
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDR command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	GMCH Graphics core rail

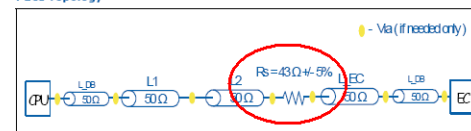
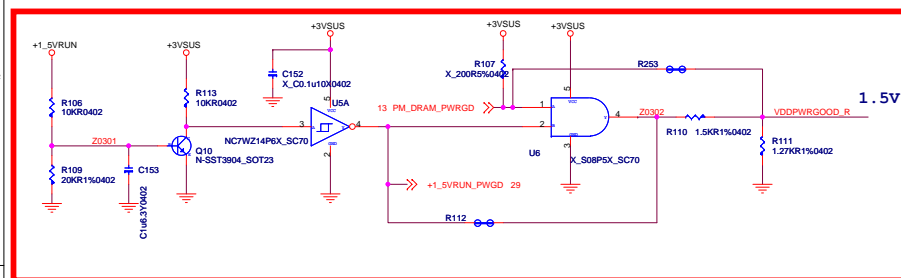
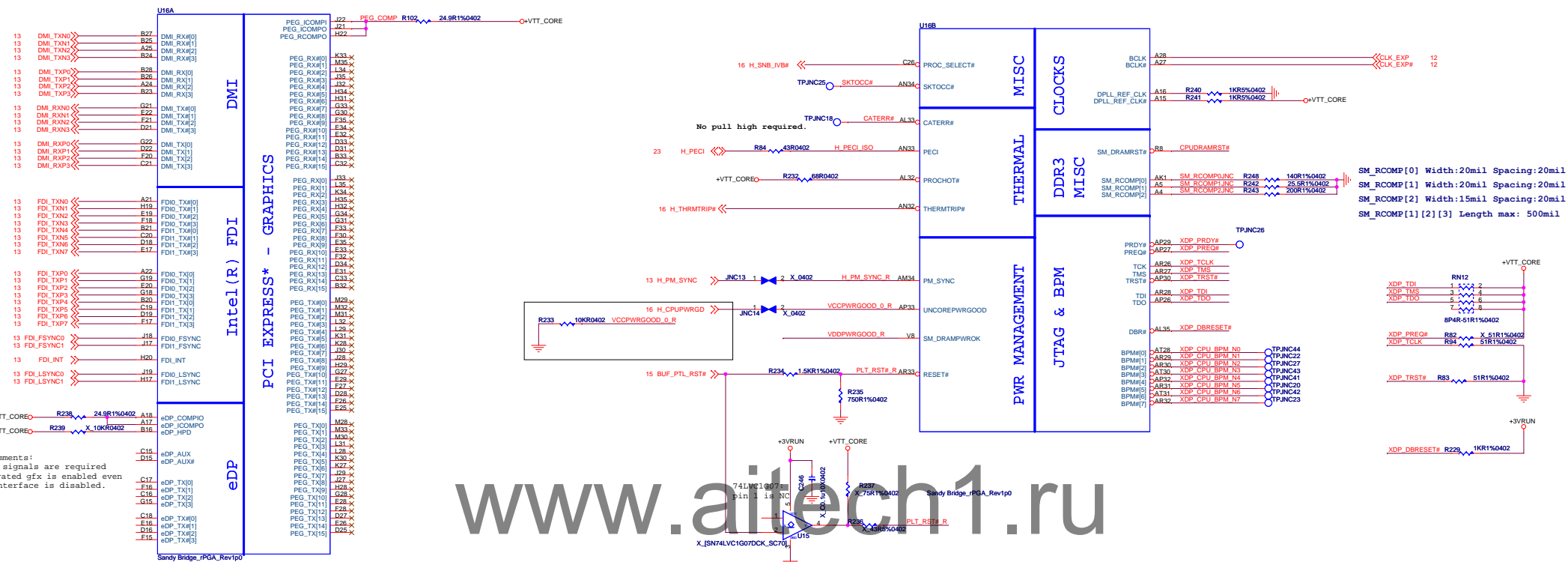
Net Naming Conventions	
Suffix	
#	= Active Low Signal
Prefix	
H	= Host
M	= DDR Memory
TP	= Test Point (does not connect anywhere else)



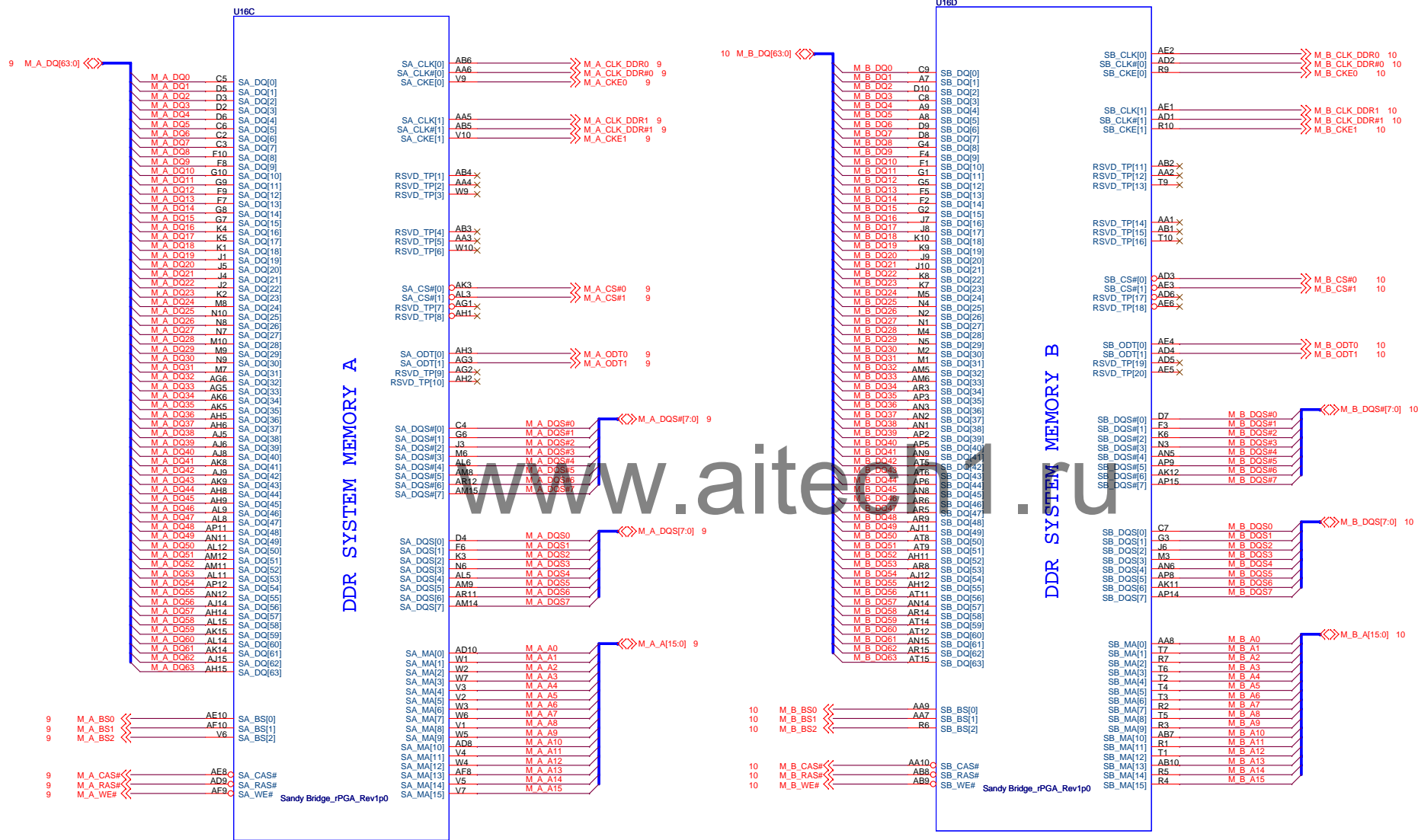
www.aitech1.ru

Power States	SLP S3#	SLP S4#	SLP S5#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	ON	OFF	OFF	OFF

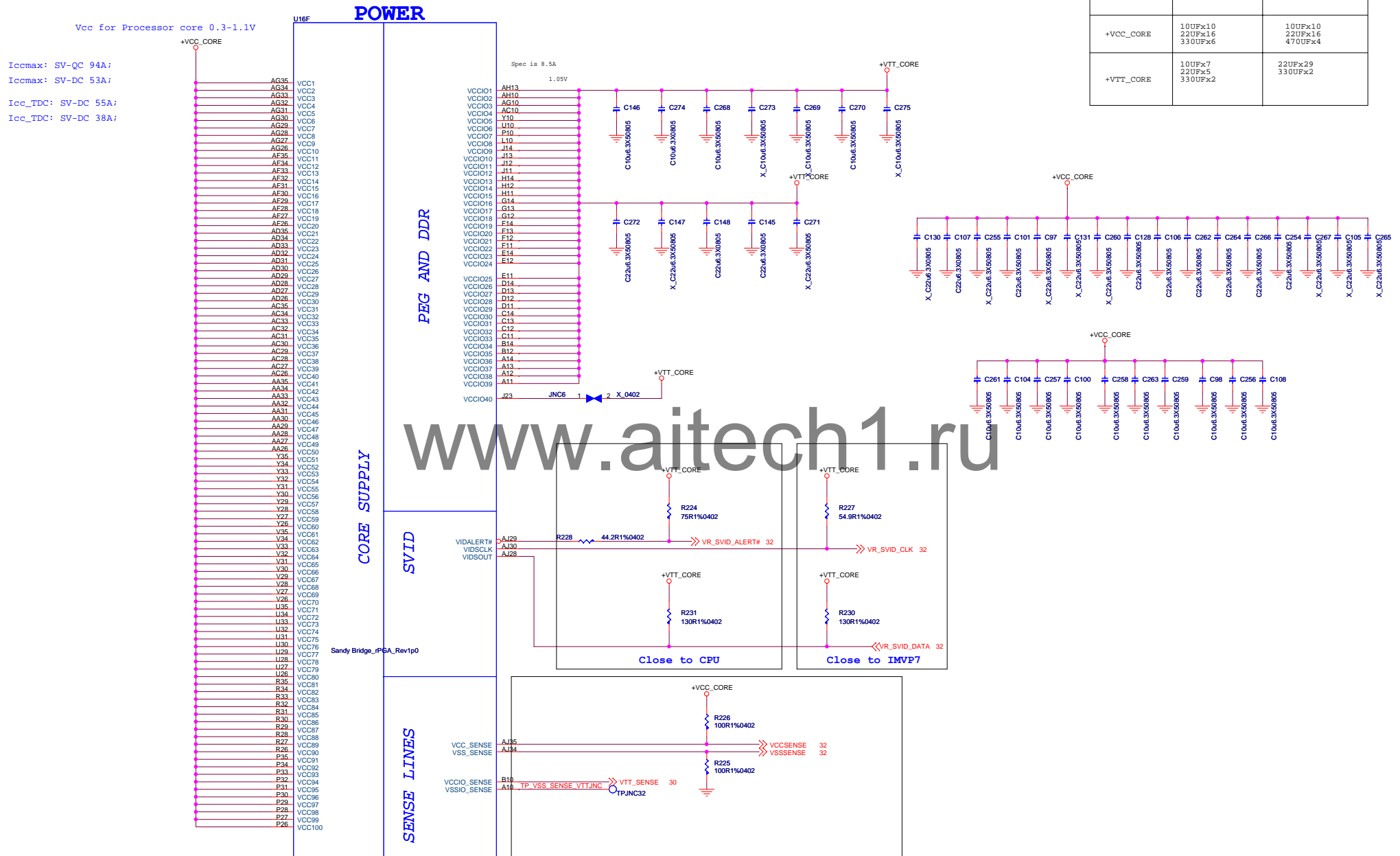
SANDYBRIDGE PROCESSOR (CLK,MISC,JTAG)



SANDYBRIDGE PROCESSOR (DDR3)

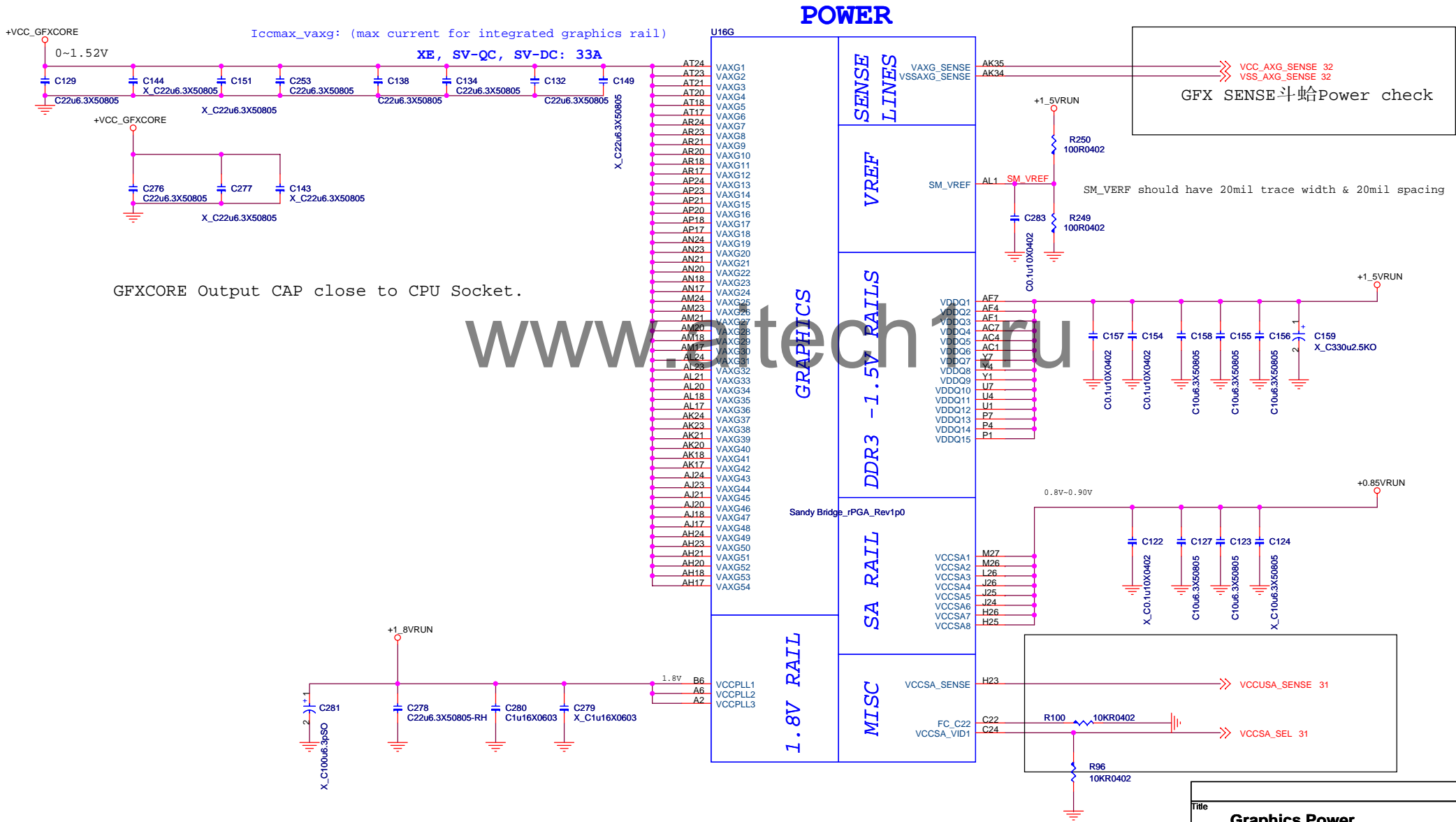


SANDYBRIDGE PROCESSOR (POWER)

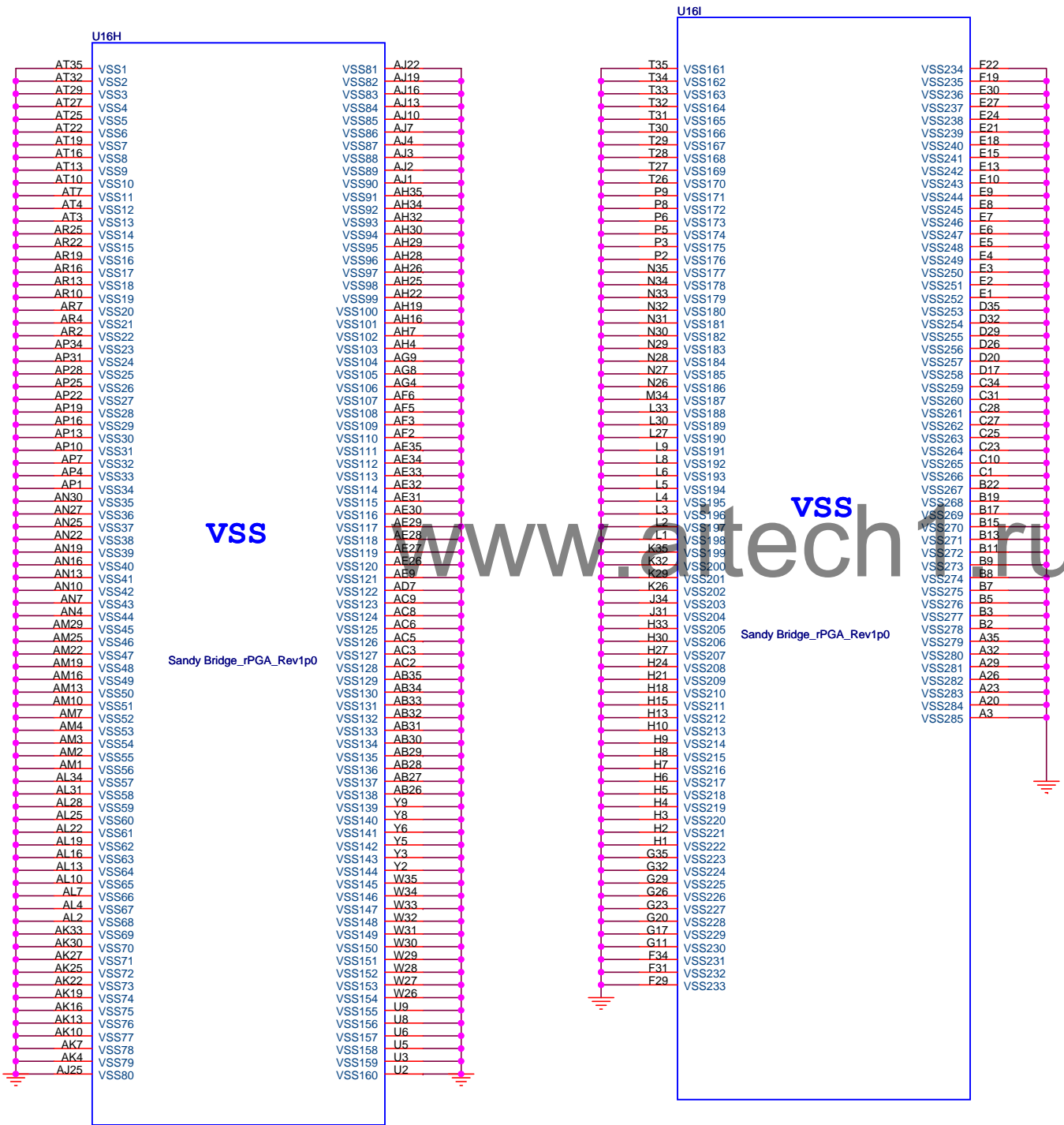


	148X schematic	CRB
+VCC_CORE	10UFx10 22UFx16 330UFx6	10UFx10 22UFx16 470UFx4
+VTT_CORE	10UFx7 22UFx5 330UFx2	22UFx29 330UFx2

SANDYBRIDGE PROCESSOR (GRAPHICS POWER)

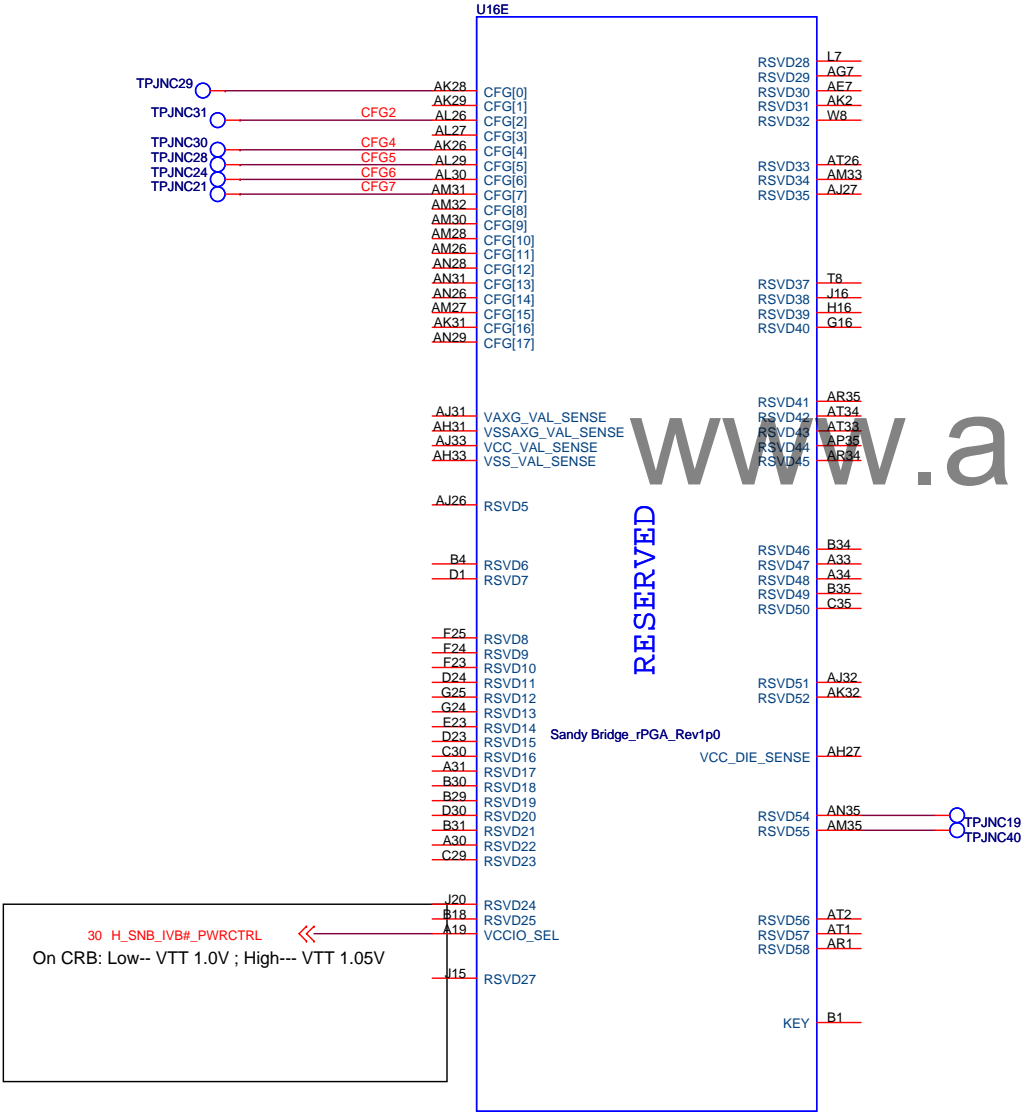


SANDYBRIDGE PROCESSOR (GND)



SANDYBRIDGE PROCESSOR (RESERVED)

The CFG signals have a default value of "1" if not terminated on the board.



CFG3 - PCI-Express Static Lane Reversal	
CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

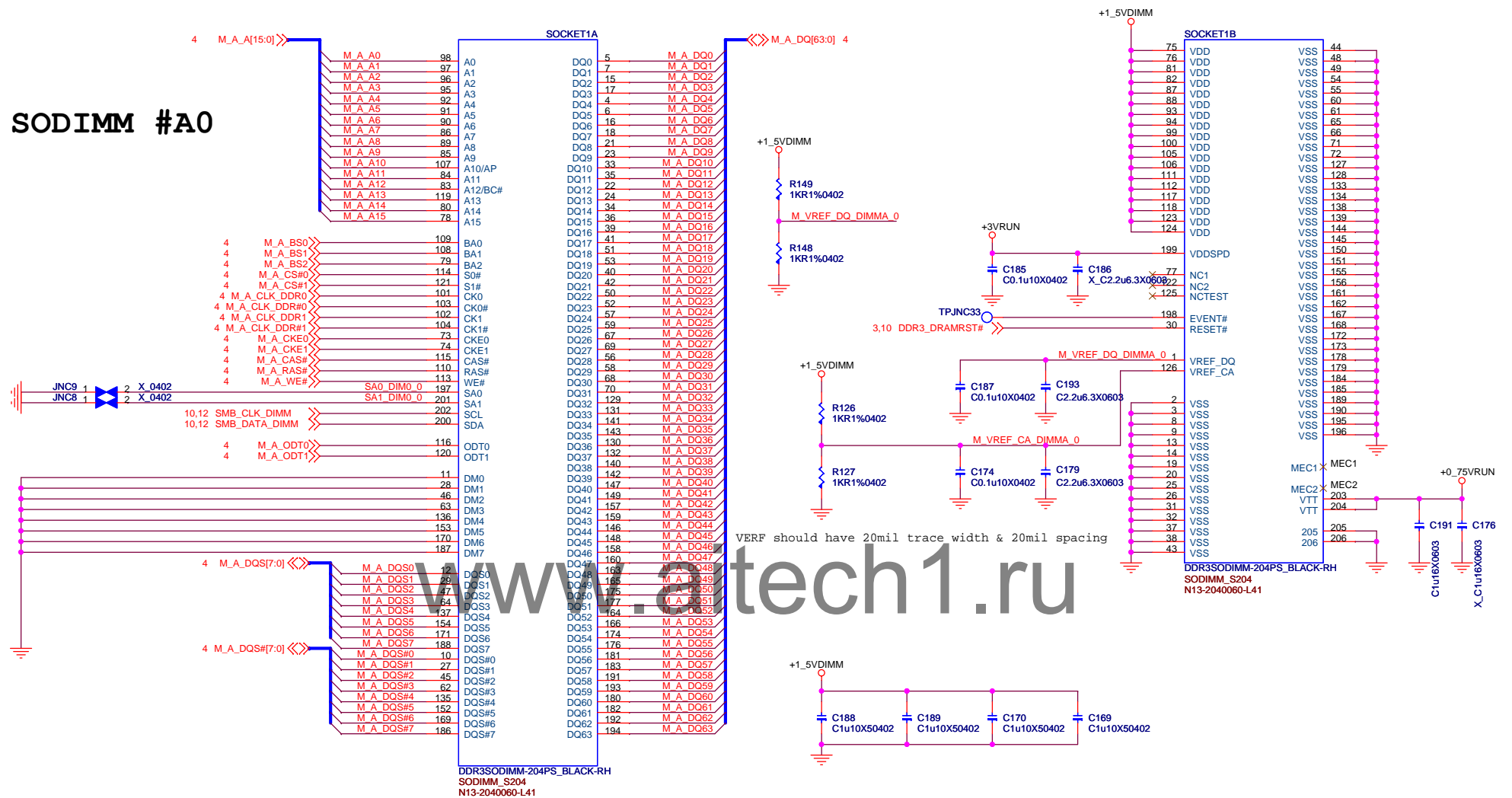
PCI-Express Configuration Select	
CFG[5:6]	11:Default X16-device 1 functions 1 and 2 disabled 10: X8 X8-device 1 functions 1 enable, function2 disabled 01:Reserved--(device 1 functions 1disabled function2 enable 00: X8 X4 X4-device 1 functions 1 and 2 enable

PEG DEFER TRAINING	
CFG7	1 : (Default)PEG train immediately following xxRESETB de assertion 0 :PEG wait for BIOS for training

DATASHEET记录	
CFG[17:7]	Reserved configuration lanes. A test point may be placed on the board for these lands.

Title		
PROCESSOR RESERVED		
Size	Document Number	Rev
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SODIMM #A0

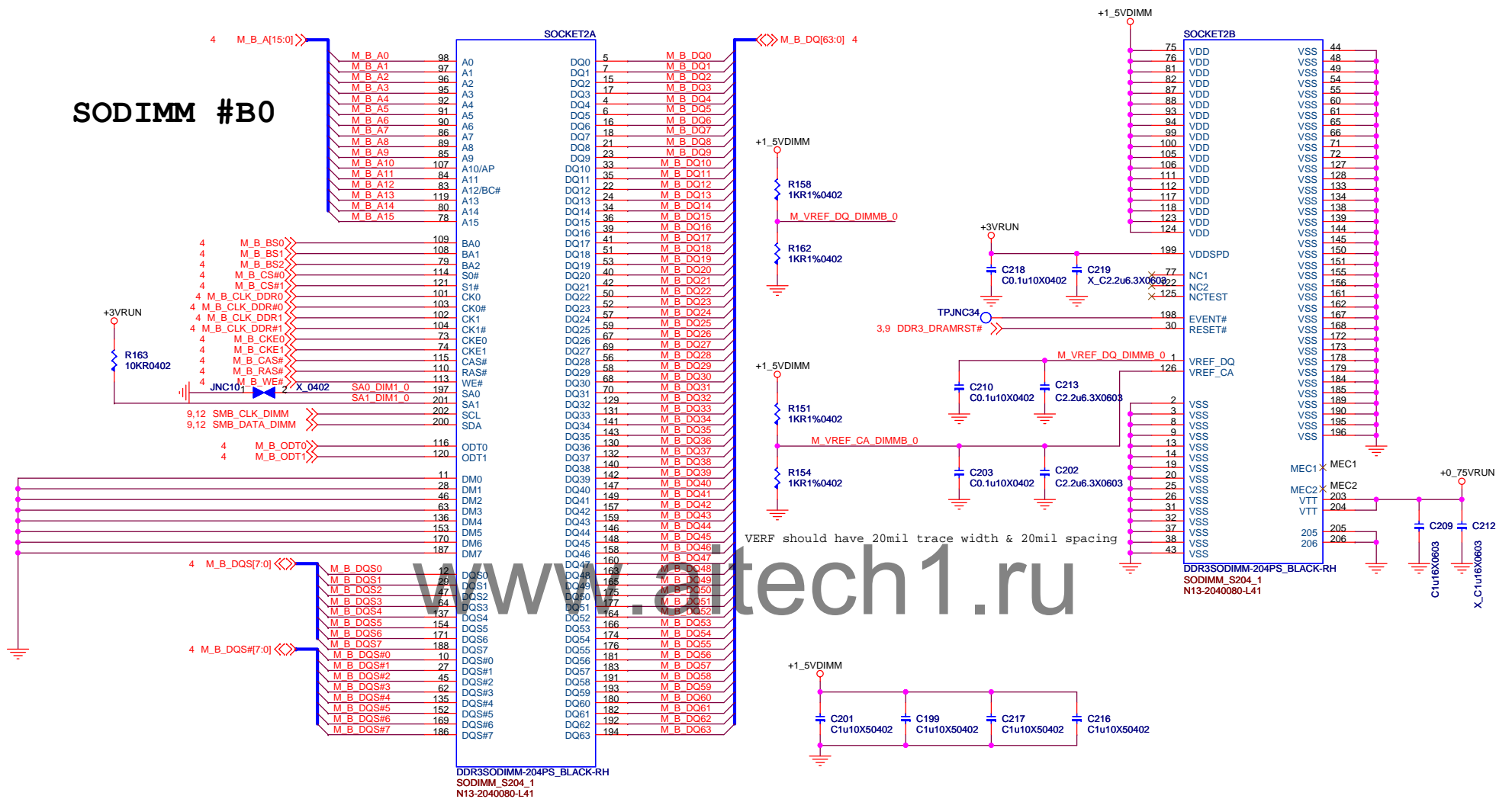


DDR3SODIMM-204PS_BLACK-RH
SODIMM_S204
N13-2040060-L41

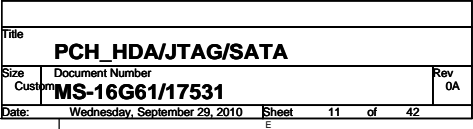
VERF should have 20mil trace width & 20mil spacing

Title				
DDR3 SODIMM A0				
Size	Document Number			Rev 0A
Custom	MS-16G61/17531			
Date:	Wednesday, September 29, 2010	Sheet	9 of 42	

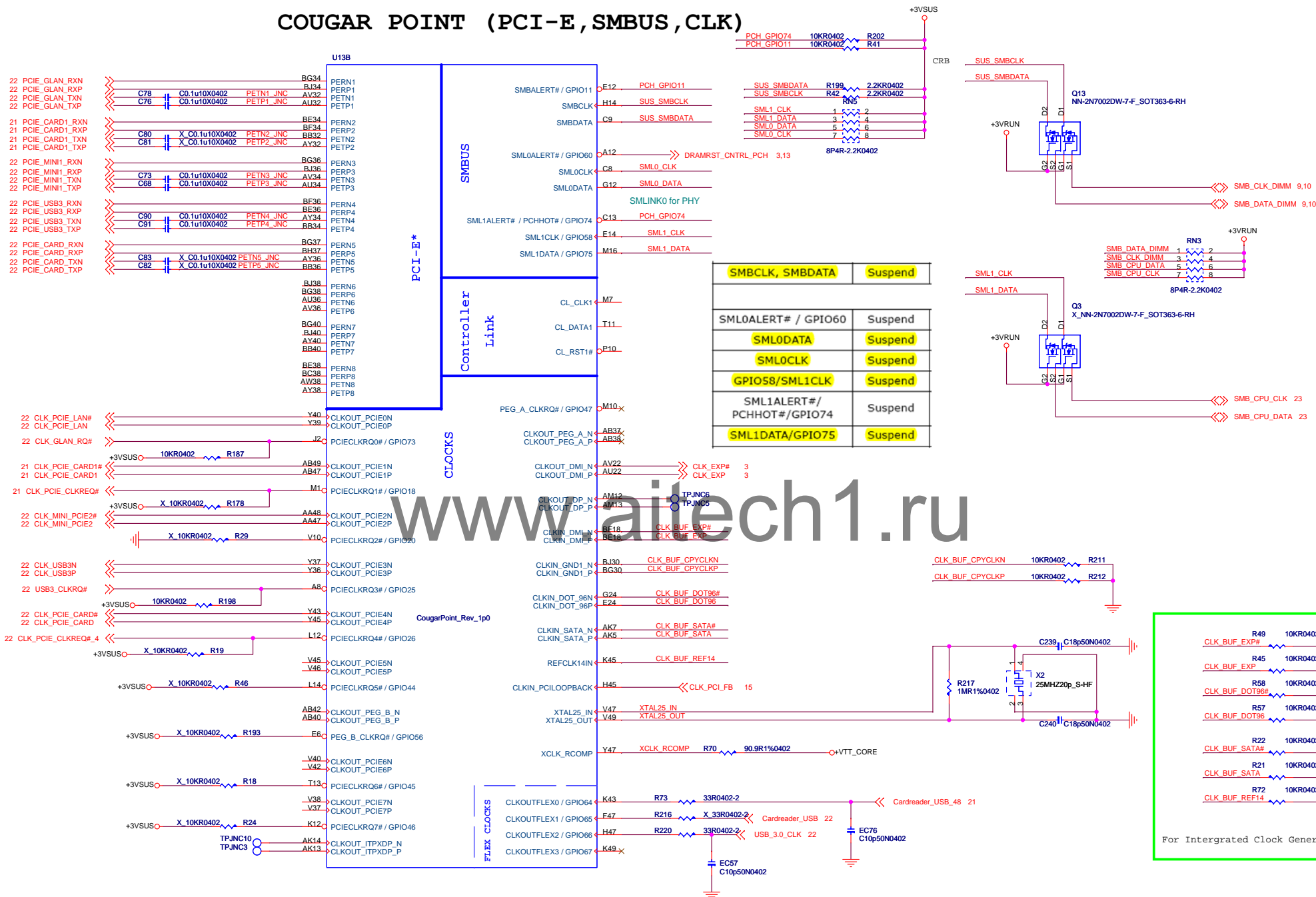
SODIMM #B0



Title			Rev	
DDR3 SODIMM B0			0A	
Size	Document Number			
Custom	MS-16G61/17531			
Date:	Wednesday, September 29, 2010	Sheet	10	of 42

[illegible]

COUGAR POINT (PCI-E, SMBUS, CLK)

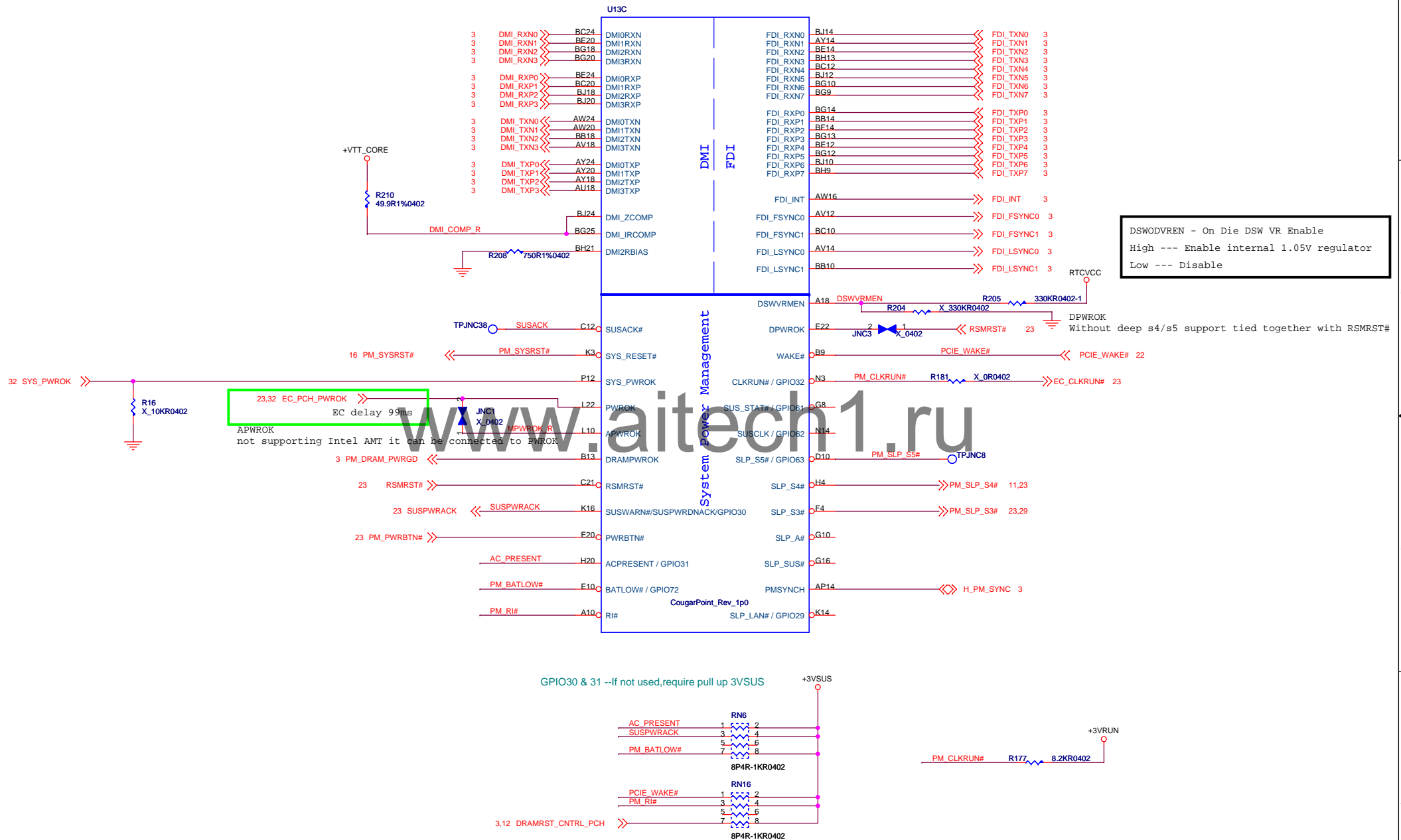


NOTE: If CLKREQ# control is not needed, say for a free running clock, do not pull-down signal to GND. This will increase leakage in Sx states. A 10 kohms±5% external pull-up resistor still needs to be used, but the corresponding CLKREQ# function can be disabled via Intel® Management Engine (Intel® ME) FW. Please refer to Intel ME FW Bring Up Guide for configuring/disabling CLKREQ#.

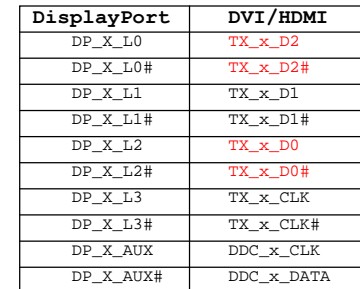
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.

File			PCH_PCIE/SMBUS/CLK
Size	Document Number	Rev	
Custom	MS-16G61/17531	0A	
Date:	Wednesday, September 29, 2010	Sheet	12 of 42

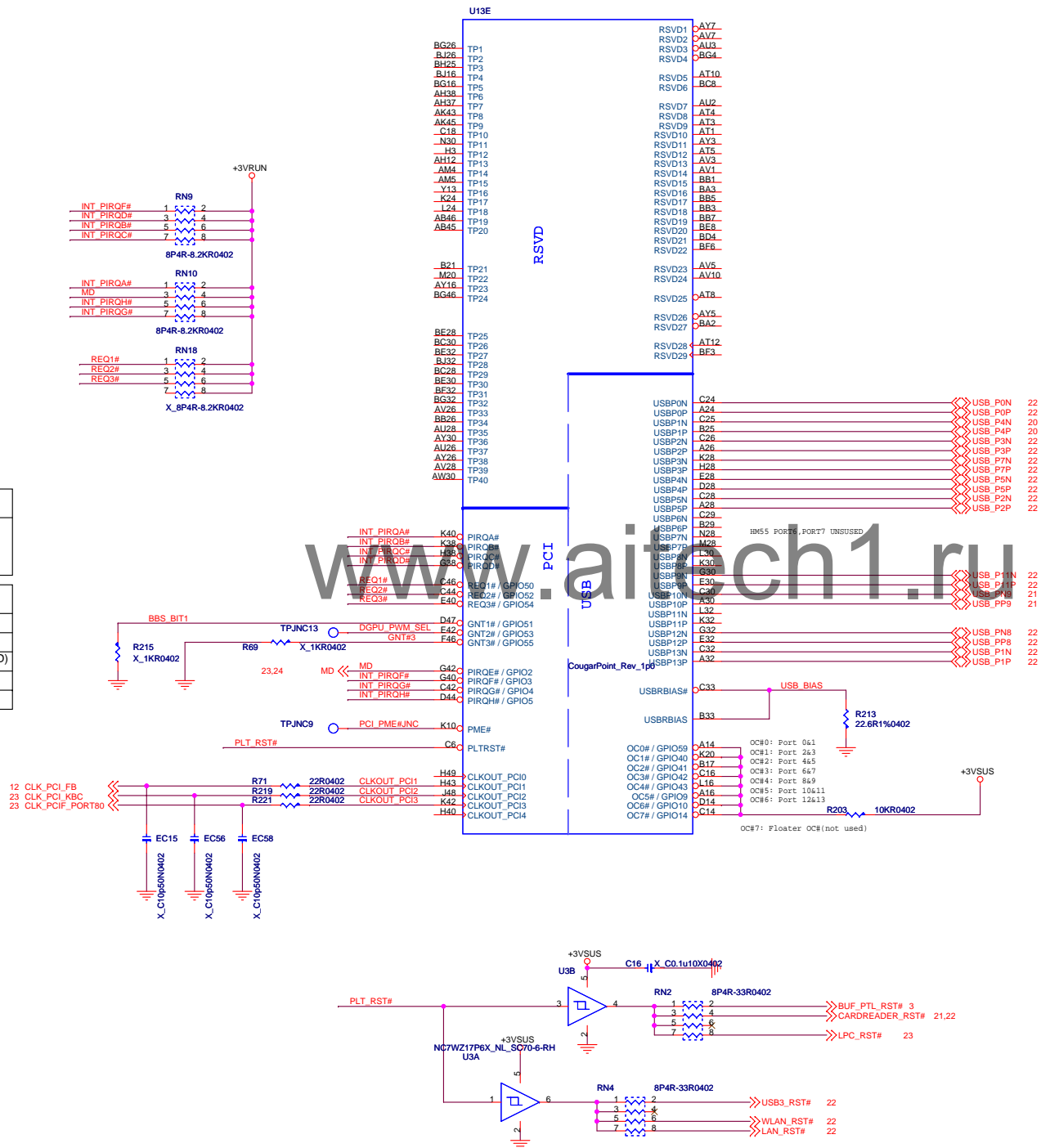
COUGAR POINT (DMI, FDI, GPIO)



AF49	LVDSB_DATA1	DDPC_2N	B447
AF47	LVDSB_DATA2	DDPC_2P	B448
AF43	LVDSB_DATA3	DDPC_3N	B447
		DDPC_3P	B449
N48	CRT_BLUE	DDPD_CTRLCLK	M43
P43	CRT_GREEN	DDPD_CTRLDATA	M36



COUGAR POINT (PCI,USB,NVRAM)



A16 swap override Strap/Top-Block Swap Override jumper	
GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	—
1	1	SPI

GPIO0 & 6 & 16 & 22 & 34 & 38 & 48 --If not used,require pull up 3V_{RUN}
GPIO57 --If not used,require pull up 3V_{SUS}
GPIO15--High is support TLS,internal pull-down
GPIO27 is deep S4 & S5 weak up event,internal pull high.& It's VCCFDIPLL internal VRM strapping pin
GPIO35 --Un- Muxed. If not used Can be NC

COUGAR POINT (GPIO,VSS_NCTF,RSVD)

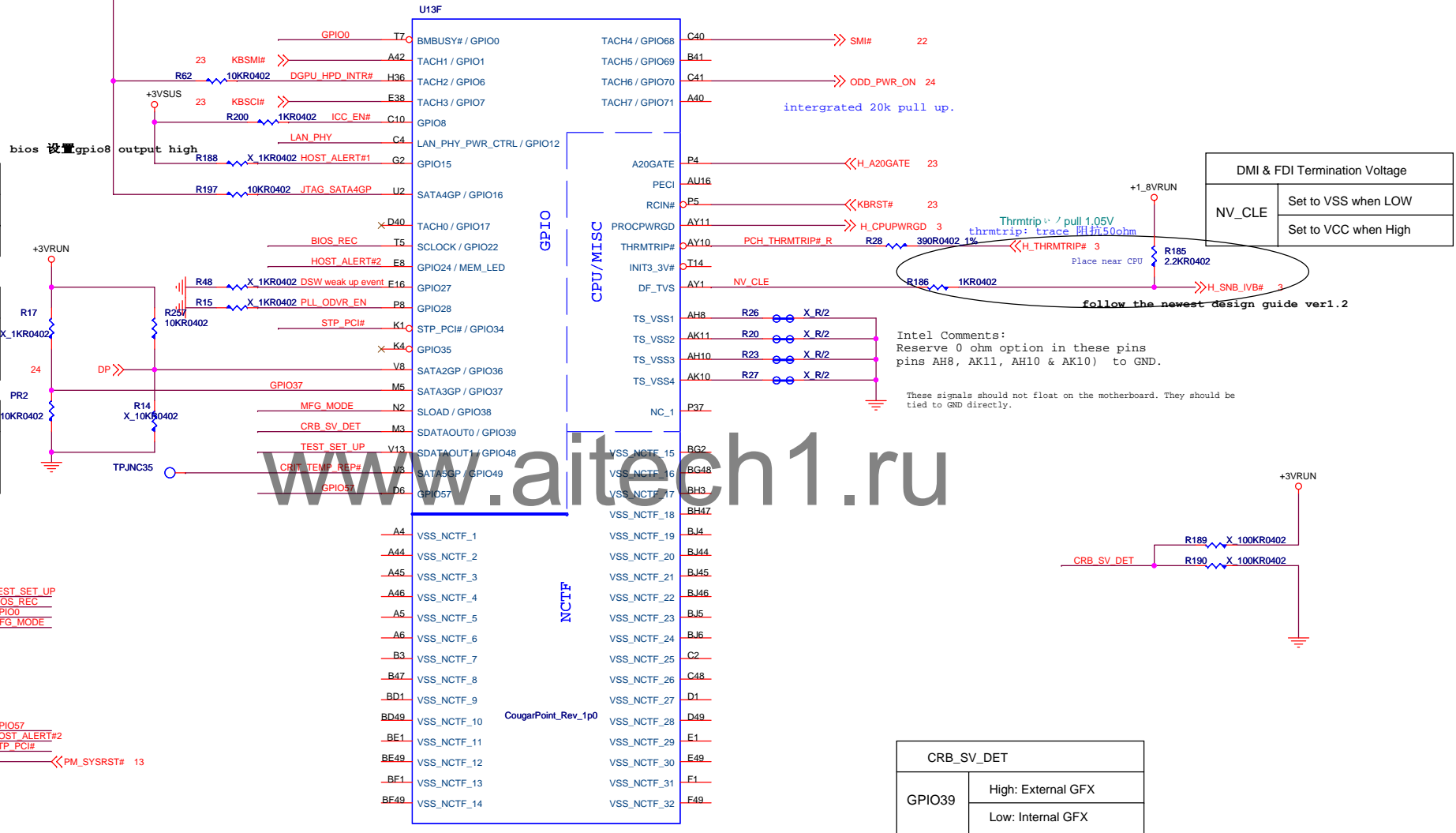
GPIO8 is no longer needed as a functional strap for Integrated clocking. Integrated Clock Enable functionality is achieved via soft-strap. The current default is Clock Enabled.

bios 设置 gpio8 output high TACH[7:0]/GPIO[71:68, 7,6,1,17,27,28] intergrated 20k pull up summer 443554 P97

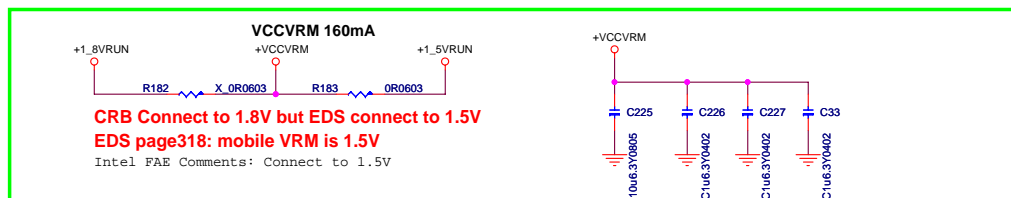
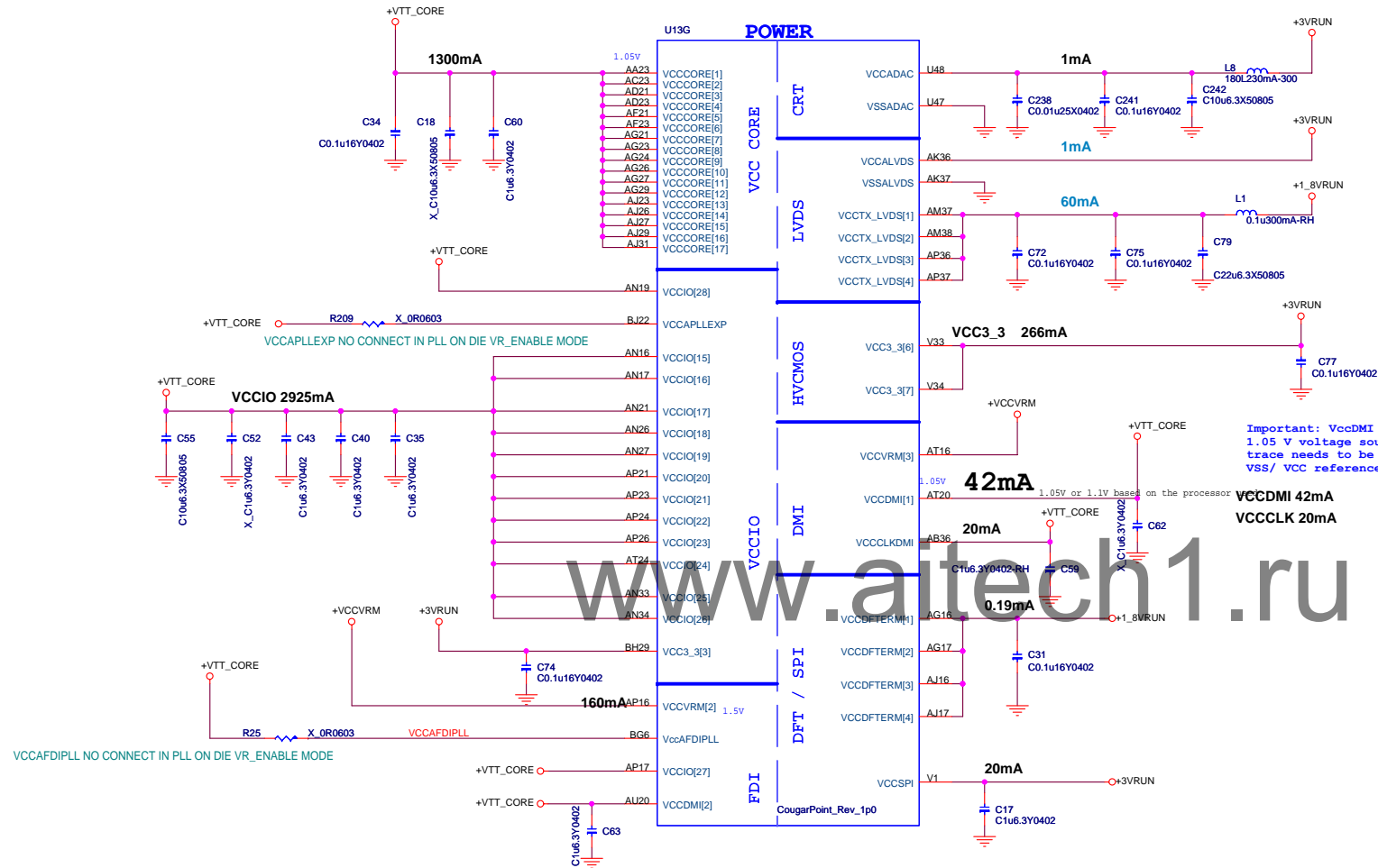
PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable) Low: Disable

DMI termination voltage override	
GPIO36	Low-- TX,RX terminated to same voltage (DC coupling mode)default

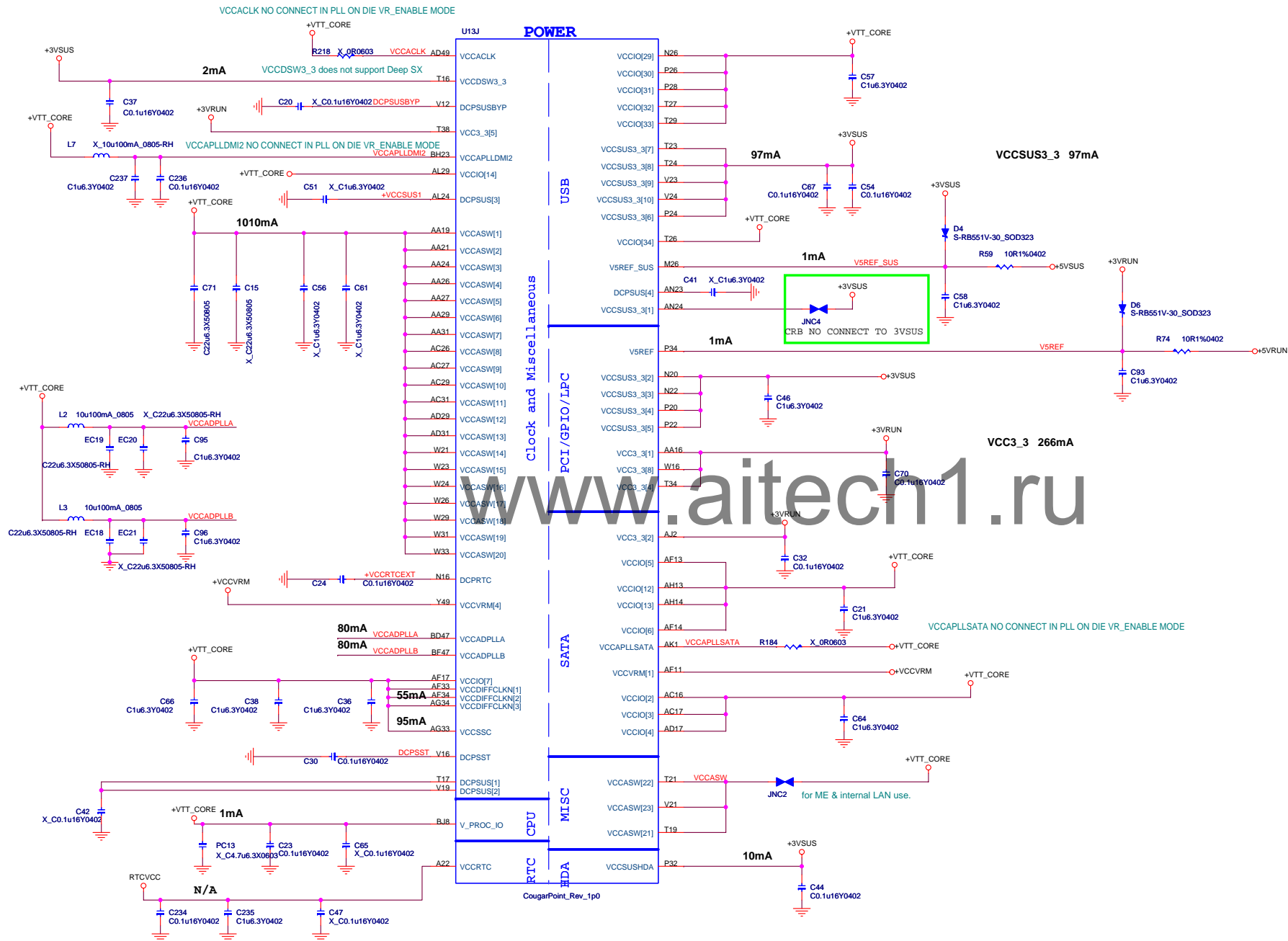
FDI termination voltage override	
GPIO37	Low-- TX,RX terminated to same voltage (DC coupling mode)default



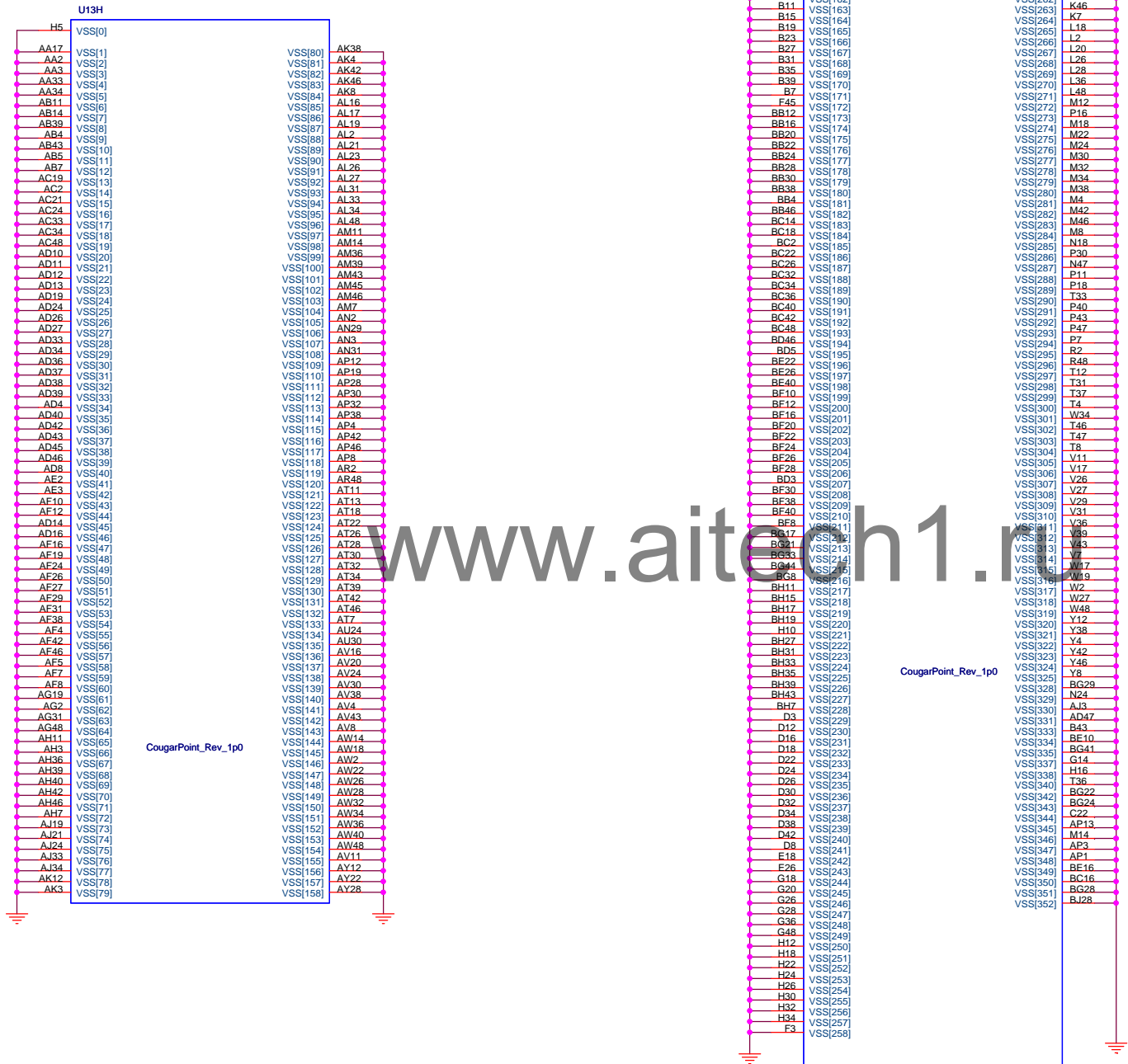
COUGAR POINT (POWER)

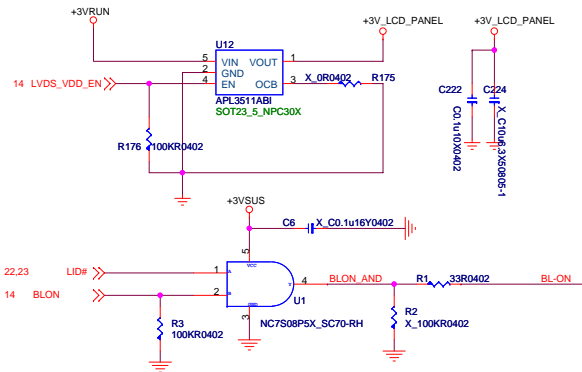


COUGAR POINT (POWER)



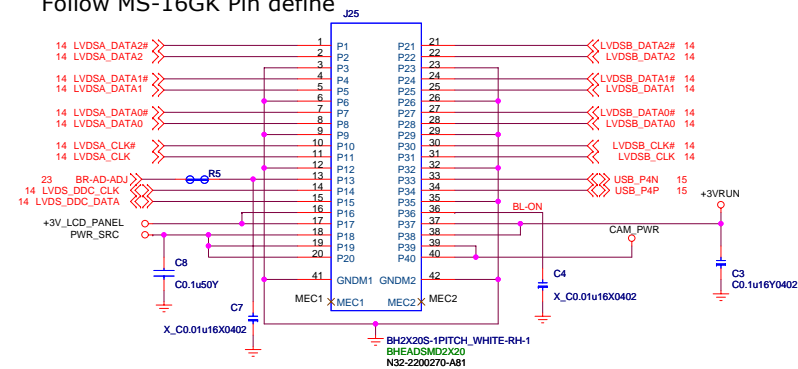
Cougar Point (GND)



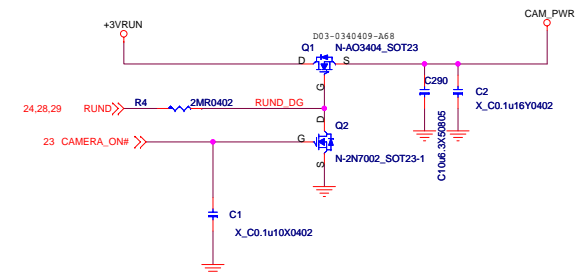


ChA . L
Follow MS-16GK Pin define

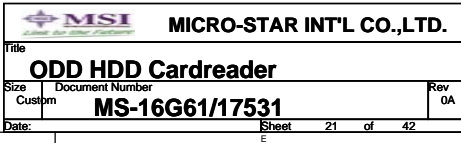
ChB . H

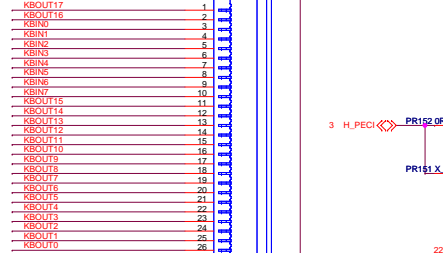


CAMERA LVDS ON

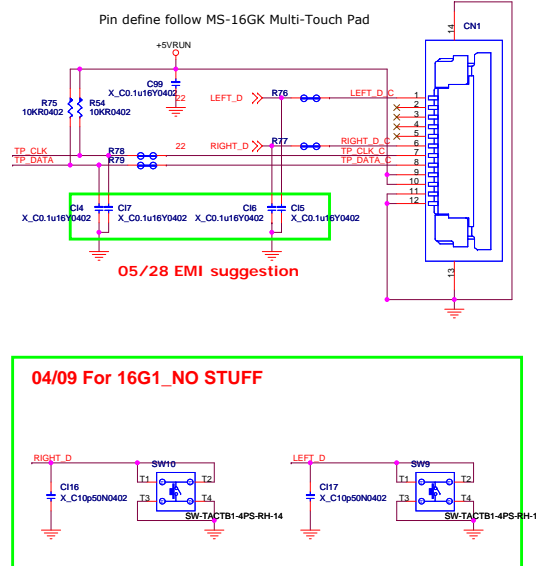
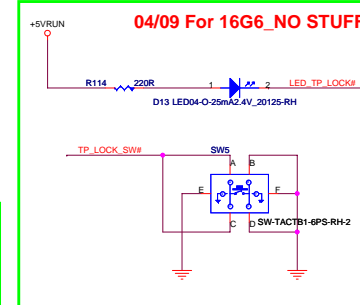
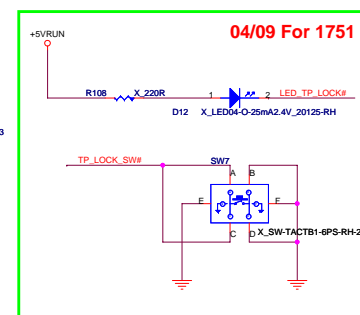
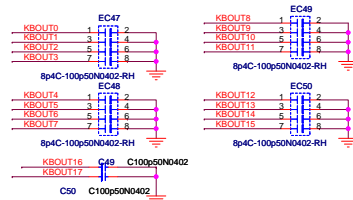
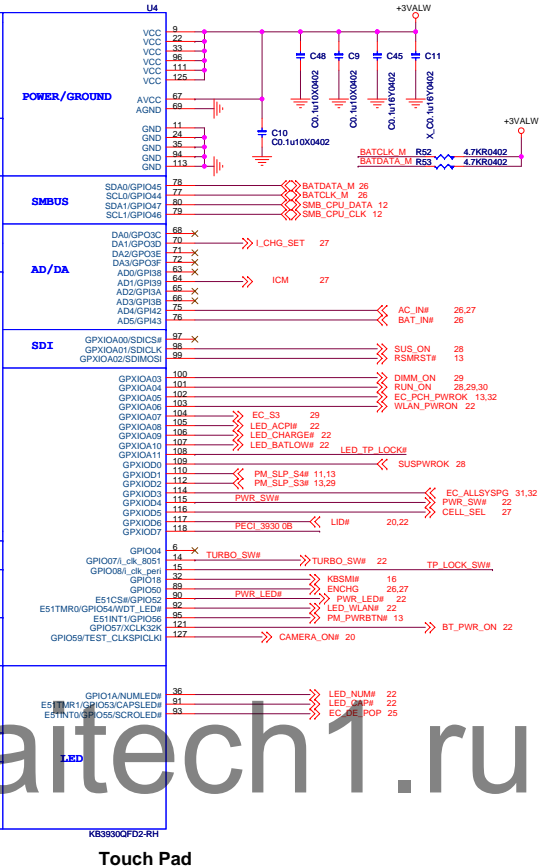
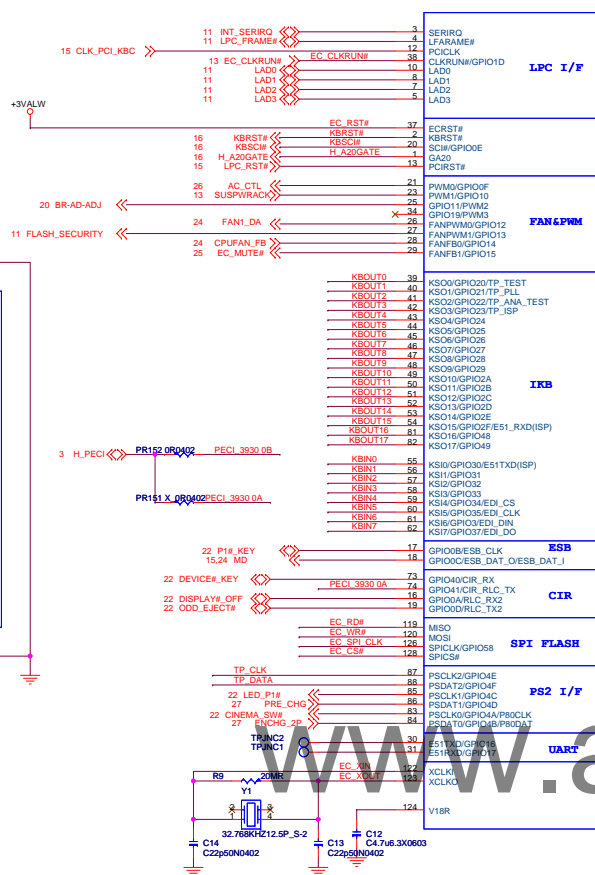
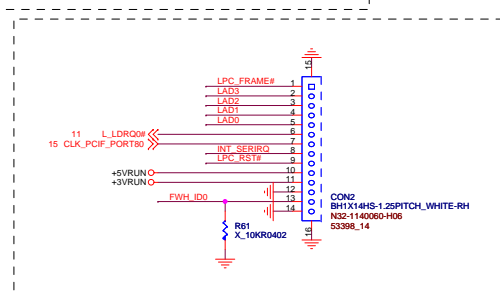
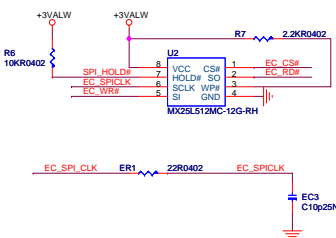


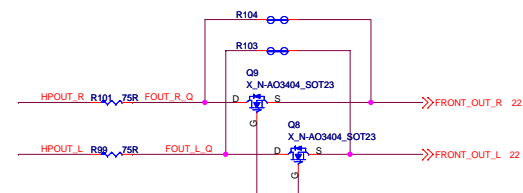
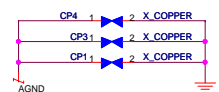
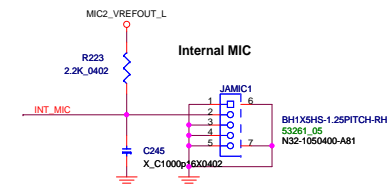
Title		
CRT/LVDS/CCD		
Size	Document Number	Rev
Custom	MS-16G61/17531	0A
Date:	Wednesday, September 29, 2010	Sheet 20 of 42



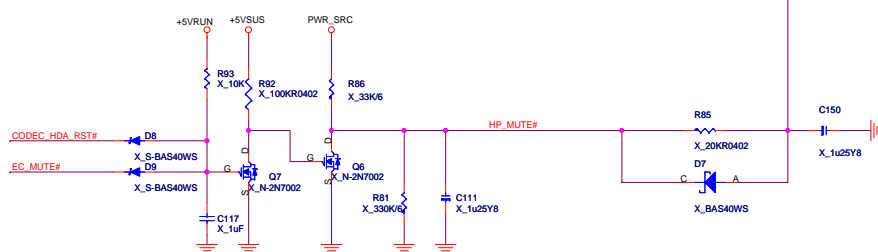


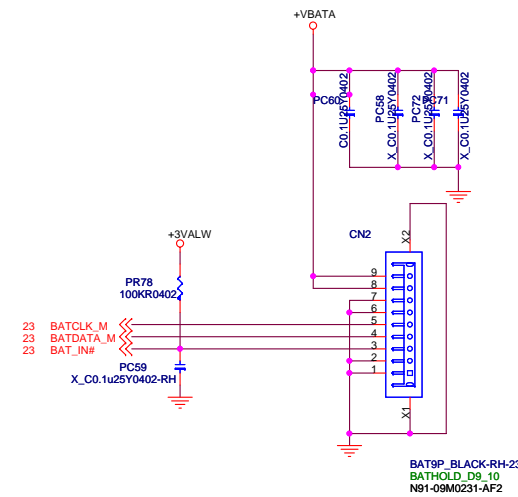
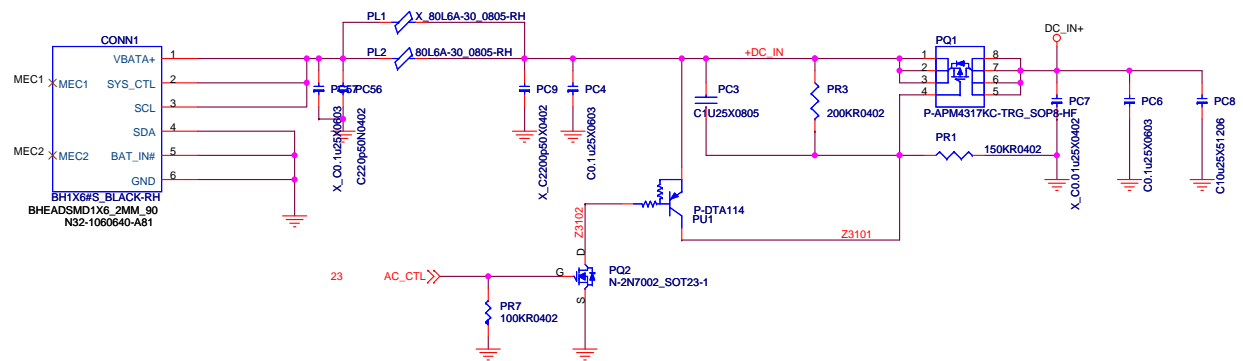
03/24 Keyboard pin define swap





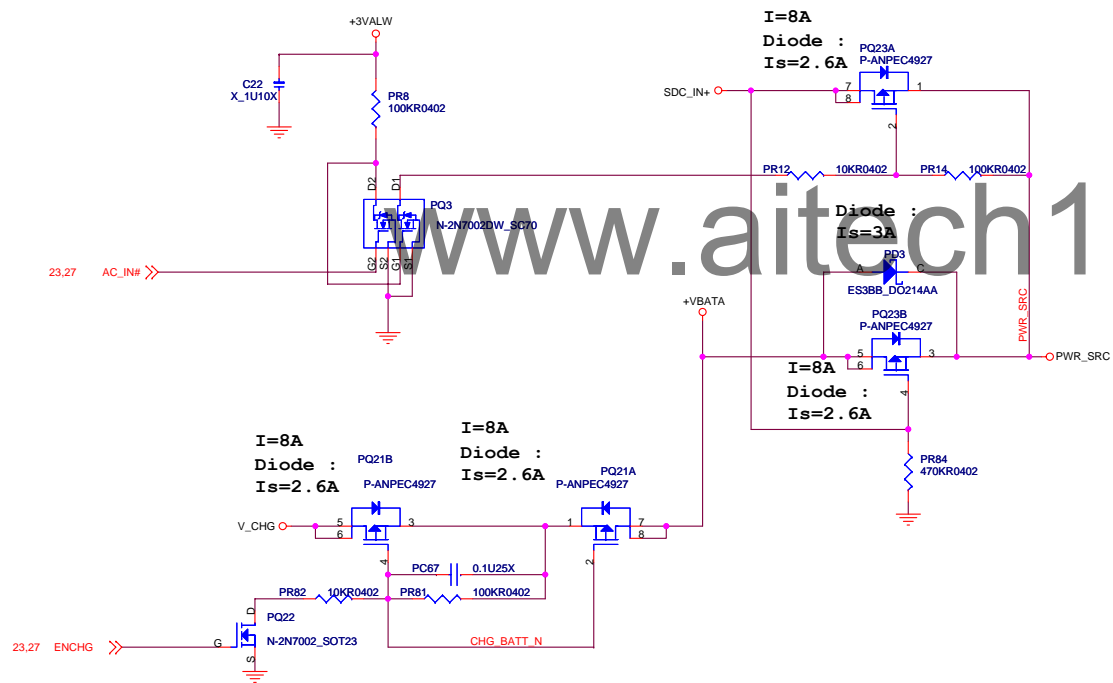
20 mil trace width is required for 40hm loading
10 mil trace width is required for 80hm loading
the trace length/ Speaker wire length of SPKL+/L-/R+/R- is same as possible as you can.

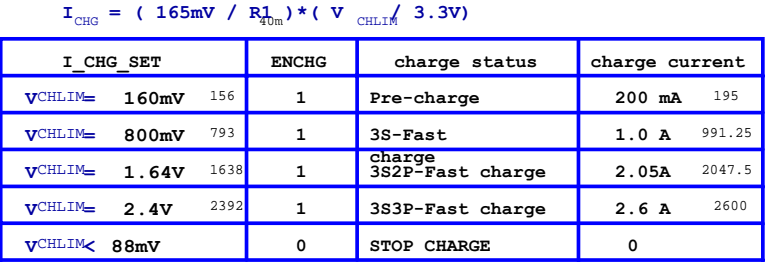




JBAT1 Pin Definition

- 1: GND
- 2: GND
- 3: BAT_IN#
- 4: SMBDATA
- 5: SMBCLK
- 6: NC
- 7: NC
- 8: VBATA+
- 9: VBATA+



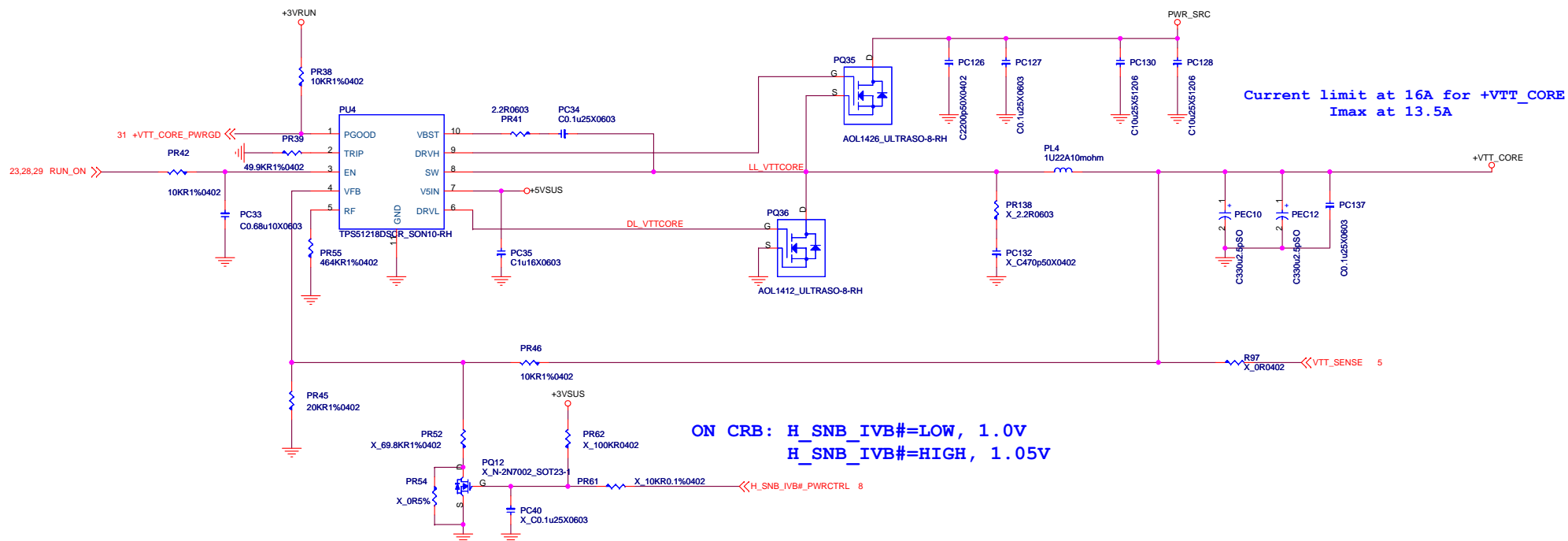


Current limit at 7A for +3VSUS
Imax at 6A

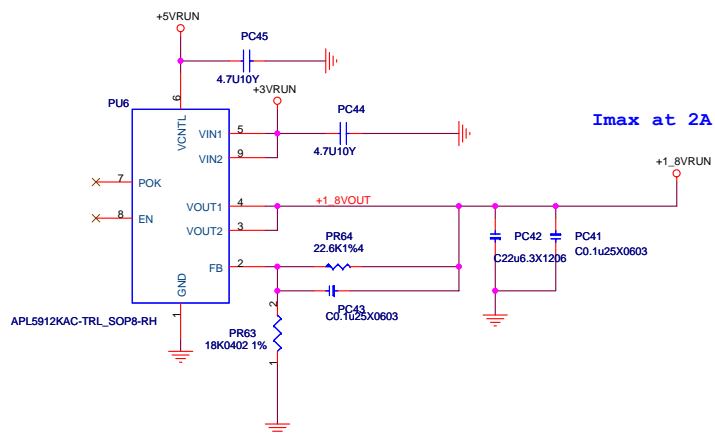
Current limit at 8A for +5VSUS
Imax at 7A

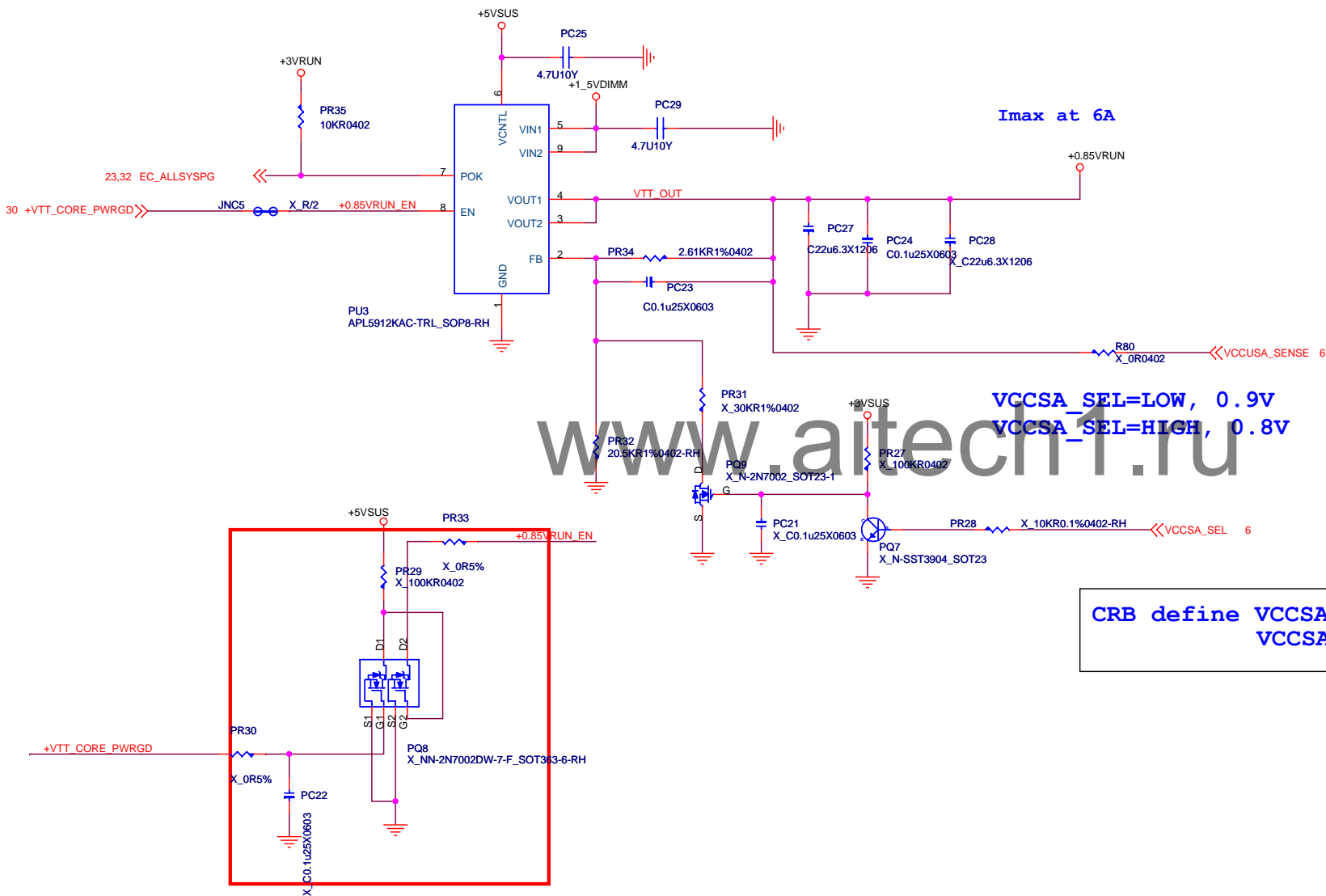
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Title		System Power	
Size	Customer	Document Number	Rev
		MS-16G61/17531	0A
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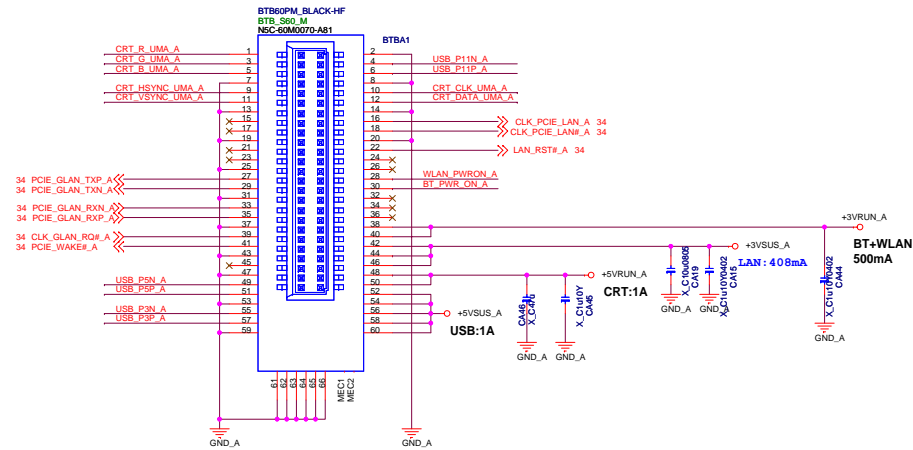
www.aitech1.ru





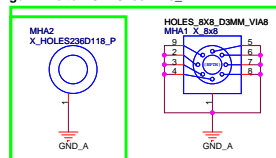
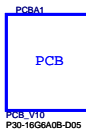
Title		
0.85V		
Size B	Document Number	Rev 0A
MS-16G61/17531		
Date:	Wednesday, September 29, 2010	Sheet 31 of 42

(凹ESATA,USB,LAN,CRT,BT+WLAN)

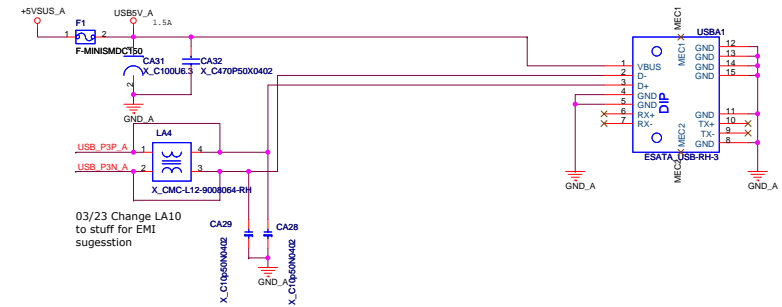
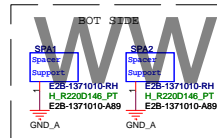


02/25 Change MHA8 to HOLES_R276D185P_PT

03/30 Change MHA8 to HOLES236D118_P

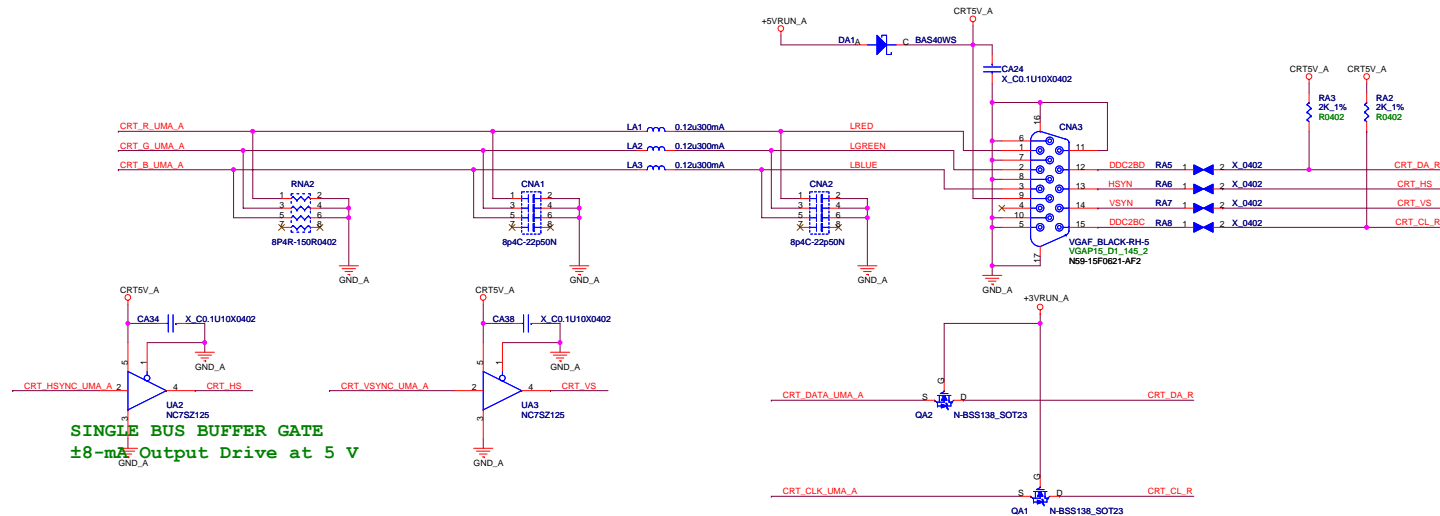


02/23 Change to 8 vias for EMI suggestion



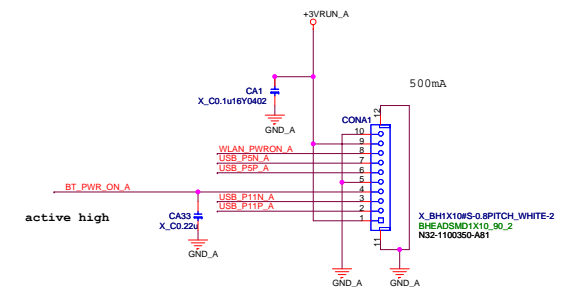
03/23 Change LA10 to stuff for EMI suggestion

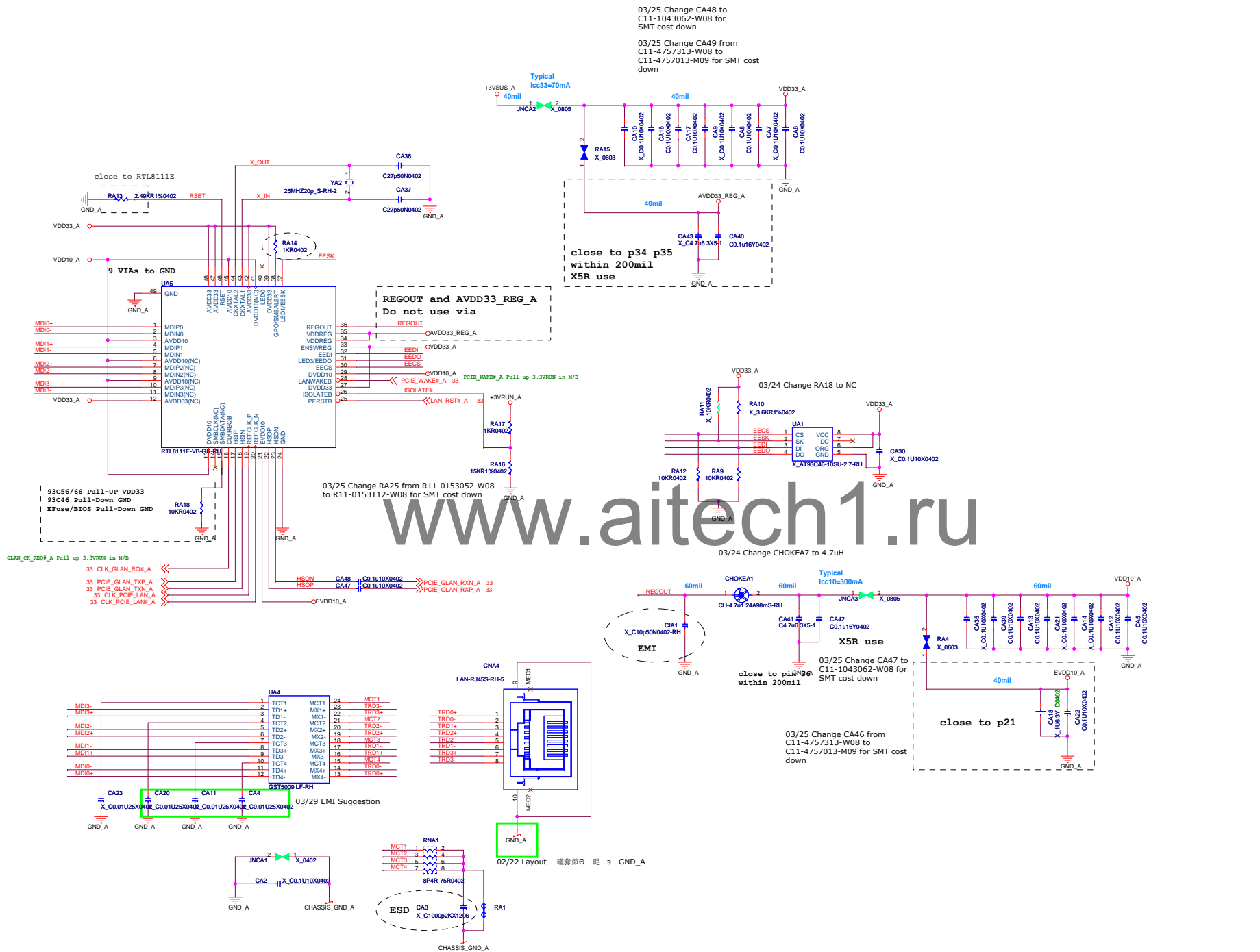
D-Sub Connector



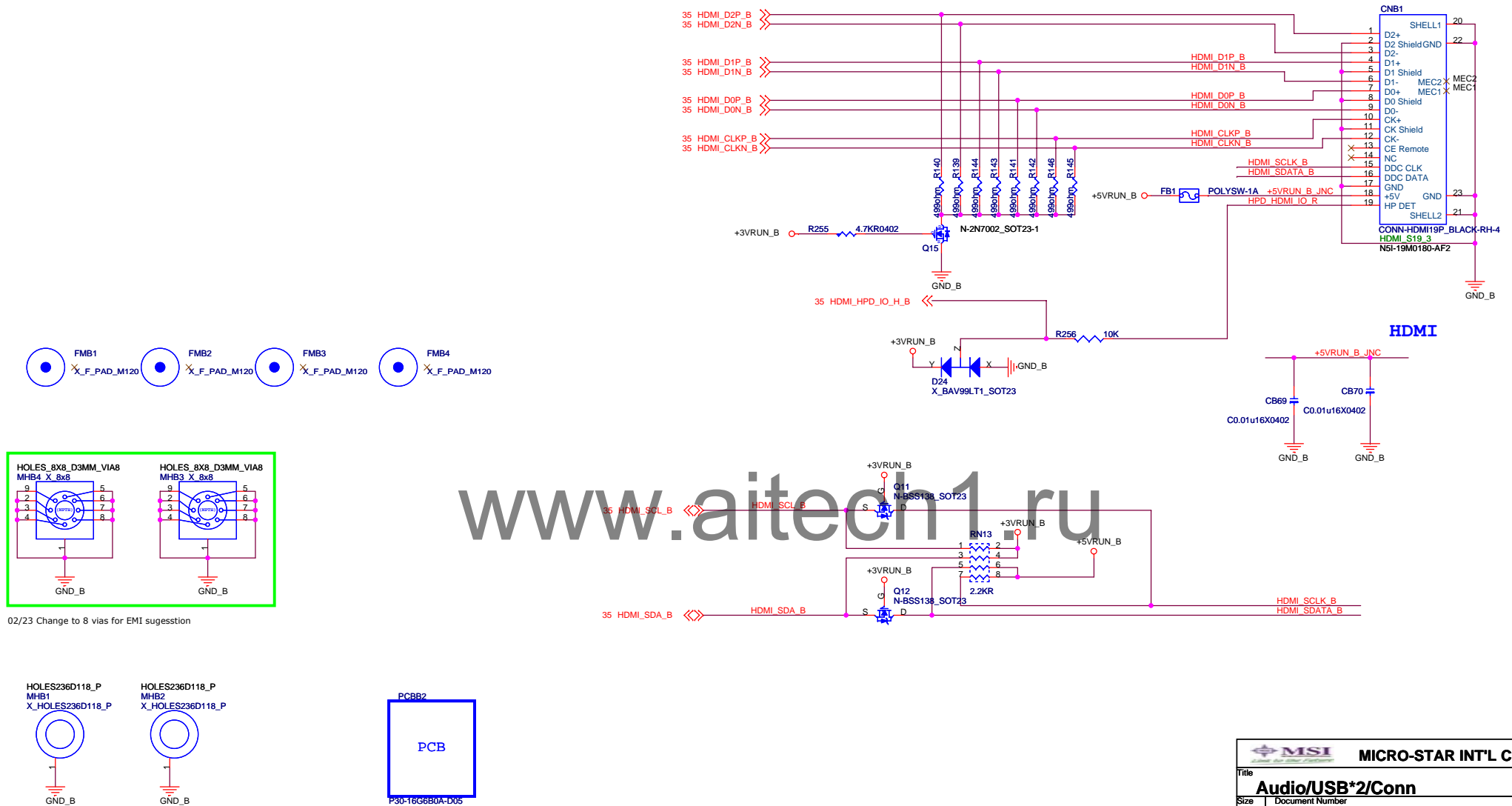
SINGLE BUS BUFFER GATE
±8-mA Output Drive at 5 V

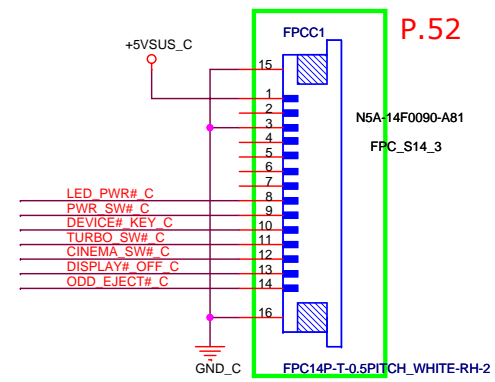
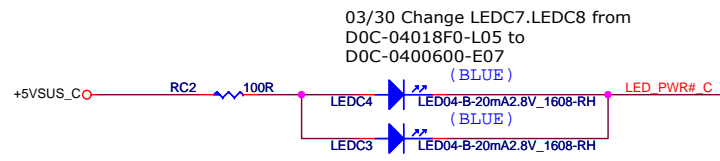
BT and WLAN Combo Connector



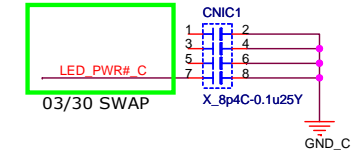
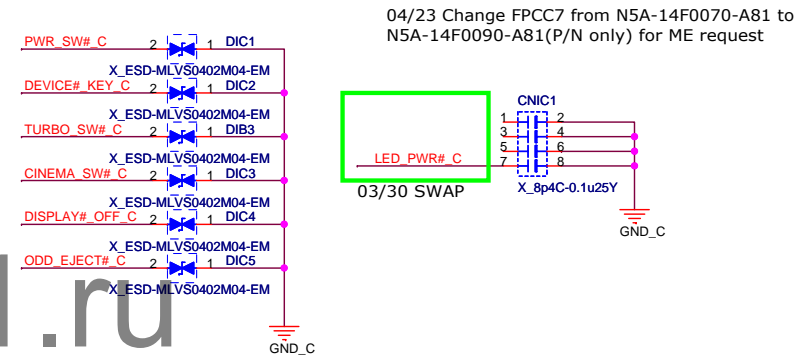
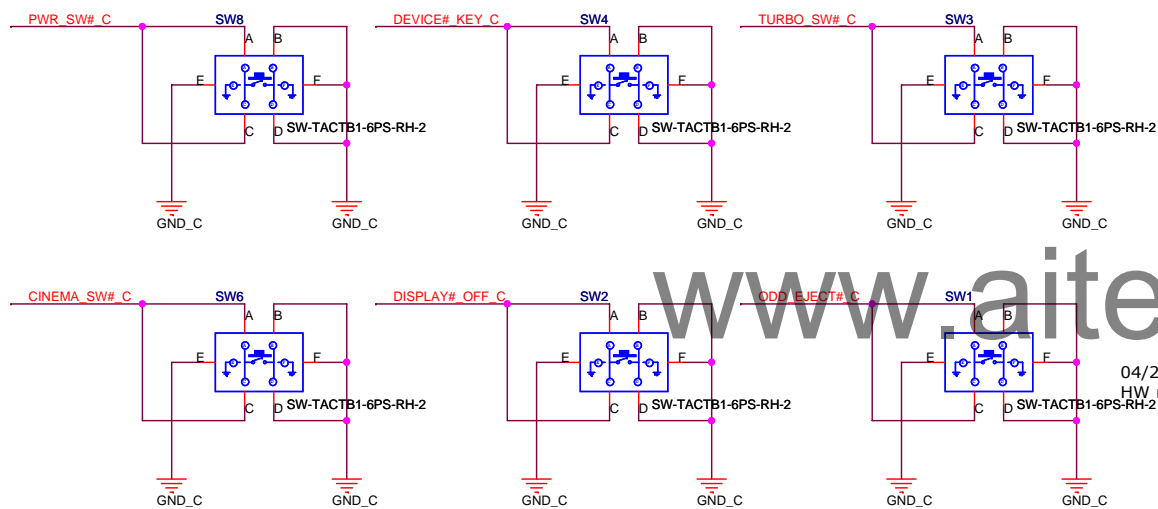


HDMI Connector



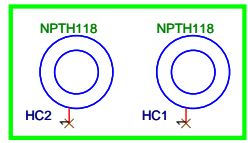
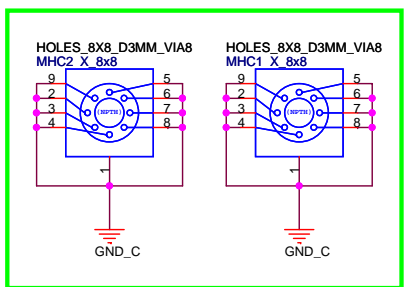


03/29 Remove ECO and Cinema LED for ID request




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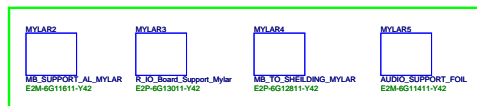
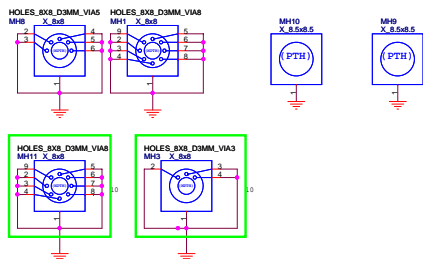
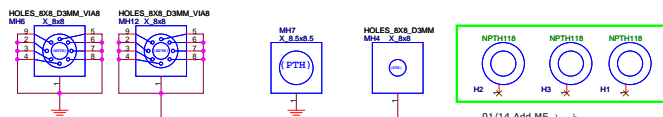
04/28 Fix SWC8's HW mismatch



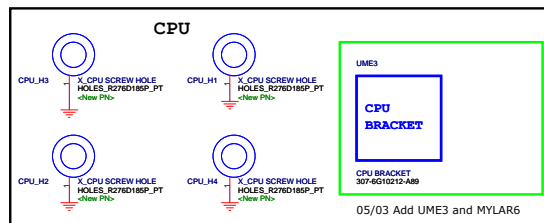
03/26 Add ME



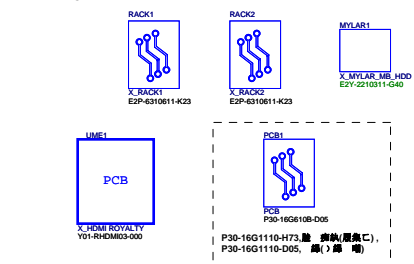
 MSI <small>Micro-Star International Co., Ltd.</small>		MICRO-STAR INT'L CO.,LTD.	
Title			
PWR SW / LED			
Size B	Document Number MS-16G61/17531		Rev 0A
Date:	Sheet	37	of 42



04/23 Add MYLAR2, MYLAR3, MYLAR4, MYLAR5 for ME request

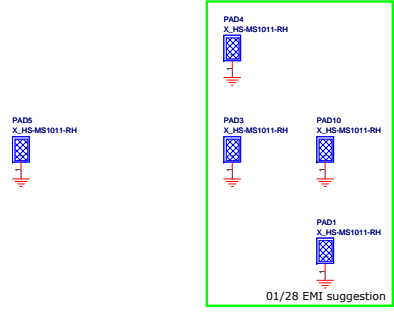


03/04 Change CPU Holes to NC

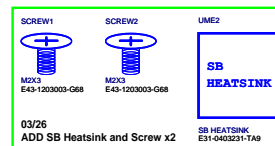


TOP SPRING

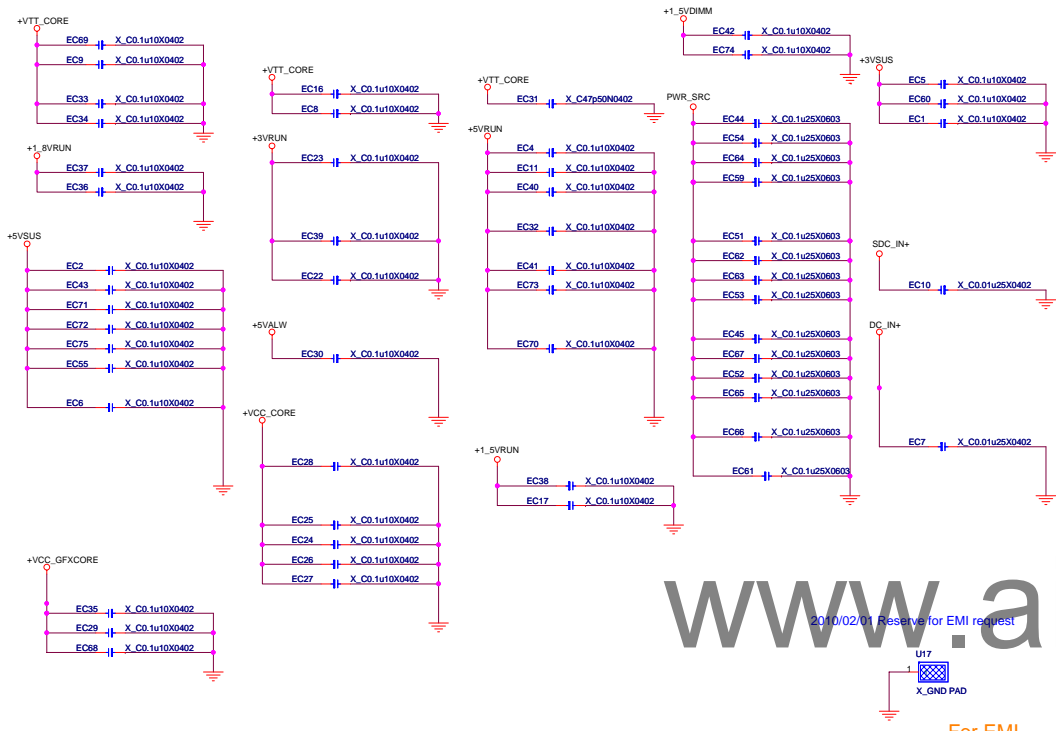
BOT SPRING



01/28 EMI suggestion



03/26
ADD SB Heatsink and Screw x2

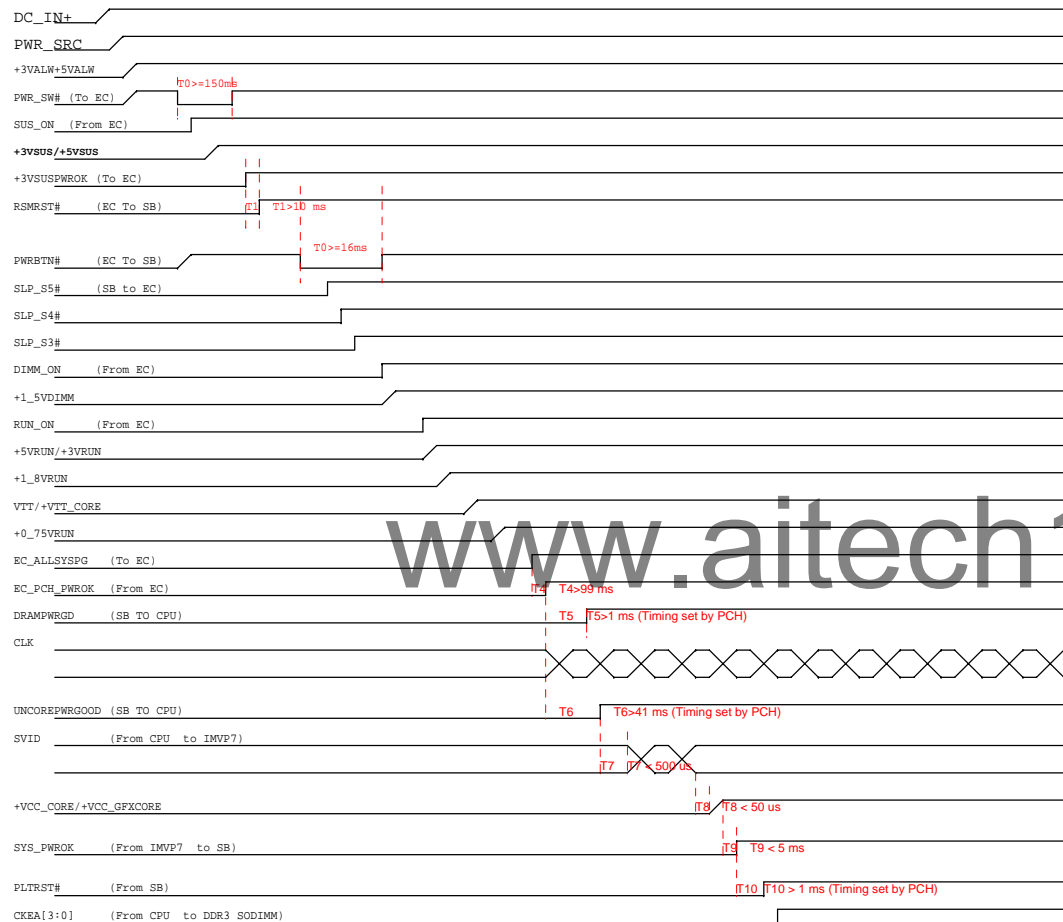


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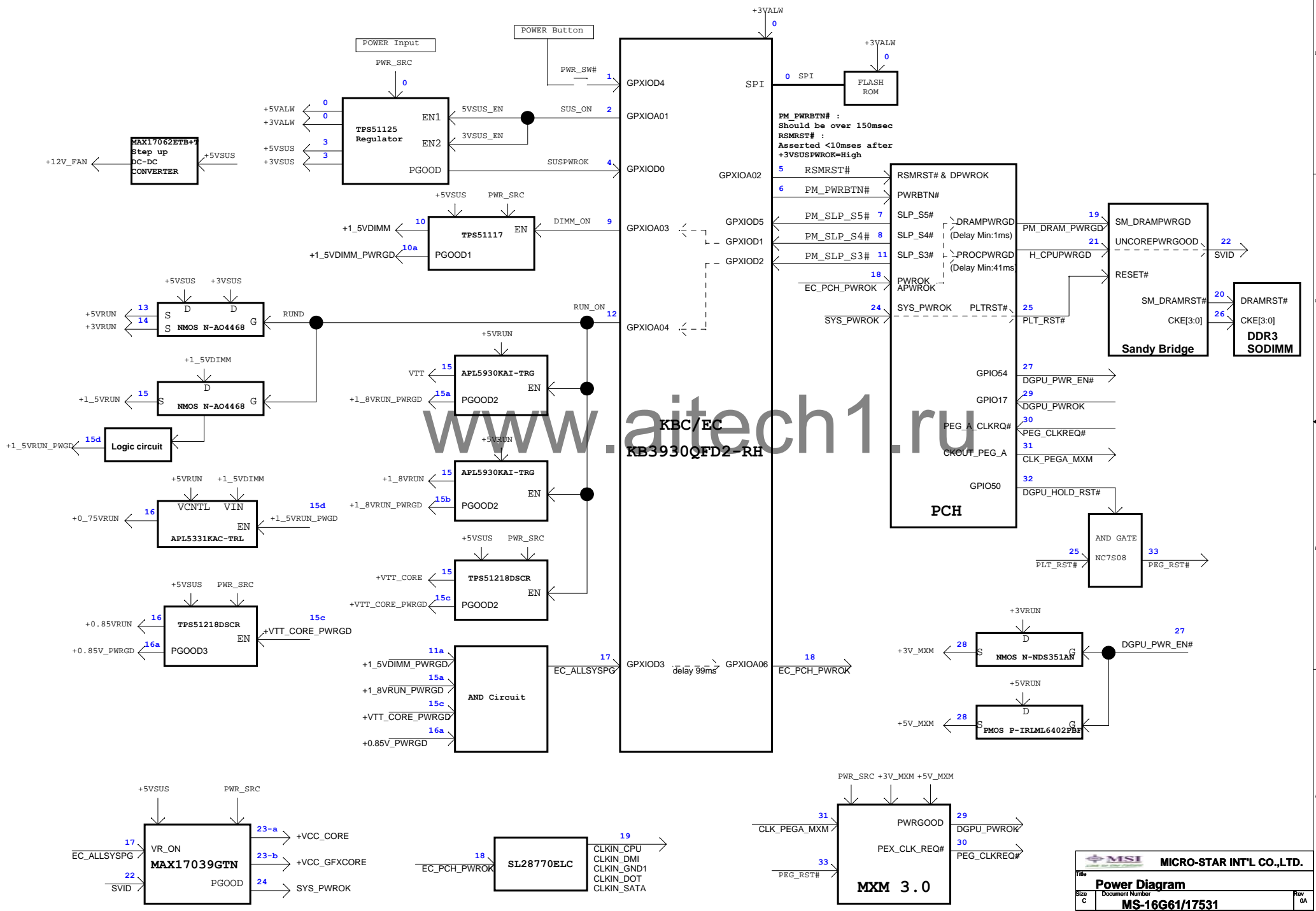
S5-S0

EC programming timing

Intel Huron River timing SPEC



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Power down Sequence DC mode S0 to G3

S0-S5

EC programming timing

Intel Huron River timing SPEC

